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Adhesion Comparison of Low Dielectric Constant Thin Films Using Four Point Bend and Nanoscratch Testing

Daniel Vilceus
University of South Florida

Adhesion Comparison of Low Dielectric Constant Thin Films Using Four Point Bend and Nanoscratch Testing

by

Daniel Vilceus

A thesis submitted in partial fulfillment
of the requirements for the degree of
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Department of Mechanical Engineering
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Major Professor: Ashok Kumar, Ph.D.
Frank Pyrtle, Ph.D.
Muhammad Rahman, Ph.D.

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DEDICATION

I dedicate this thesis to the Lord and my family, especially my loving parents Joseph M. and Marie C. Vilceus. I owe every achievement of my life to my parents, brothers and sister. I am extremely grateful for the continuous mentoring, encouragement and love they have provided throughout my life.

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Daniel Vilceus

ABSTRACT

As the semiconductor technology moves further into scaled down device structures, modern day complexities in the fabrication processes become more prevalent. This thesis focuses on the issues associated with mechaincal and adhesion failure in low dielectric constant (low-k) thin films. In this thesis the four point bend test and nanoscratch test method was used for evaluating adhesion of boro-phosphate-silicate glass (BPSG) and tetraethylorthosilicate (TEOS) low-k thin films to silicon subtrates. Nanoindation tests were also performed on the low-k films to evaluate material properties such as hardness and elastic modulus. The sample preparation and testing set up for the four point bend test and nanoscratch test were observed to be greatly disparate. Nanoscratch and nanoindentation sample preparation and sample testing were able to be carried out much quicker than in four point bending. It was observed that nanoscratch testing holds an immense potential for reducing the time needed to evaluate thin film adhesion then in FPB testing.

Nanoindentation performed on the BPSG and TEOS dielectric thin films showed uniform mechinacal properties throughout the surface of the films. The adhesion energy for BPSG and TEOS using FPB testing ranged from 29.5390 J/m^2 - 3.0379 J/m^2. While the adhesion energy for BPSG and TEOS using nanoscratch testing ranged from 0.0012 J/m^2 - 0.0028 J/m^2. It was observed that the difference in adhesion energy for FPB and nanoscratch testing was due to differing failures modes.

CHAPTER 1: INTRODUCTION

1.1 Manufacturing goals of integrated circuits

In 1975 Gordon Moore stated that the projected number of transistors that can be fabricated on a very large scale integrated (VLSI) chip would double every 18 months (Moore, 1975). His projection is now known is Moore's Law. Figure 1.1 below shows the projected trend of transistor increase per chip area through 2010.

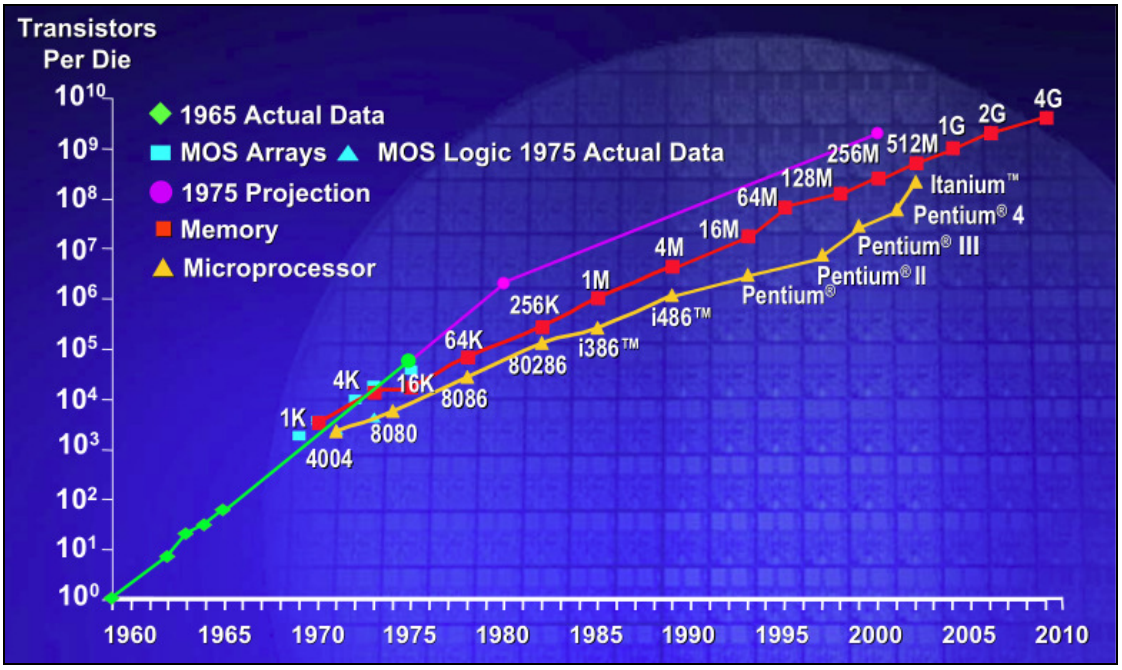

Figure 1.1 Transistors per chip area vs. years of electronic advances (Moore, 2003)

The main focus of the semiconductor industry is to continue to meet the projected transistor growth described in Moore's Law until Moore's Law cannot be sustained and meets a physical fundamental barrier.

1.2 Multilayer structures

One method of packing more transistors per area in a chip is to stack planes of transistors on top of each other. The transistor stack illustrated in Figure 1.2 is a multilayer metallization (MLM) structure. In MLM structures each plane of transistors is isolated by a dielectric capping layer that prevents electrical signal propagation between neighboring planes. The planes in MLM structures are connected to each other by wiring that goes through wholes in the dielectric capping layer.

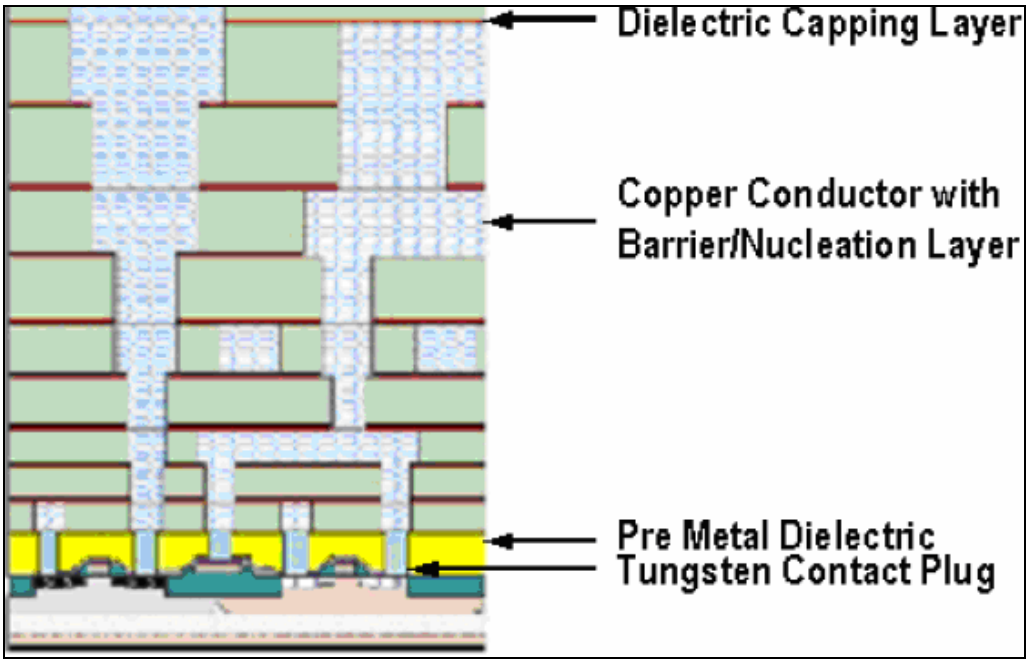

Figure 1.2 Schematic of an MLM structure (Lee, 2003)

1.3 Chemical mechanical planarization (CMP)

Chemical mechanical planarization (CMP) is the method that is universally accepted to planarize surfaces during fabrication of MLM structures. Compared to conventional planarization technologies such as bias sputtering and dry etching processes, CMP offers more versatility, simplicity and better global planarization. Figure 1.3 shows how surfaces are planarized using the CMP process. During the CMP process, the surface to be planarized is held at pressure against a rotating polishing pad soaked by abrasive based slurry.

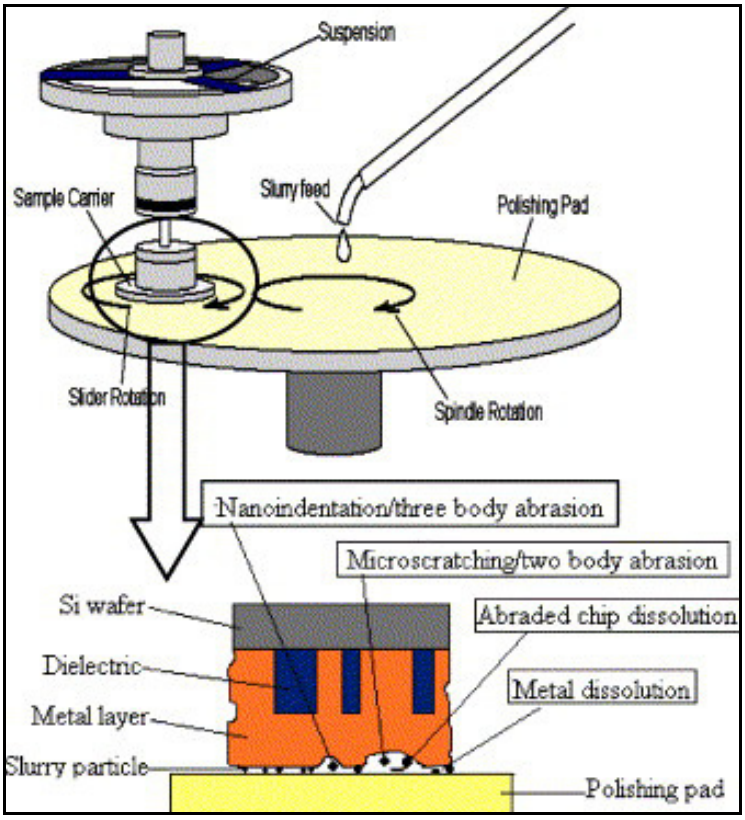

Figure 1.3 Schematic of wafer planarization by CMP process (Zantye, 2005)

1.4 Failure and reliability issues in MLM structure fabrication during CMP

During the CMP process, MLM structures experience a multitude of forces as each transistor plane and dielectric capping layer is planarized. These forces are often the cause of device failure through delamination of the dielectric capping layer. Figure 1.4 below shows the delamination of dielectric capping layers during CMP.

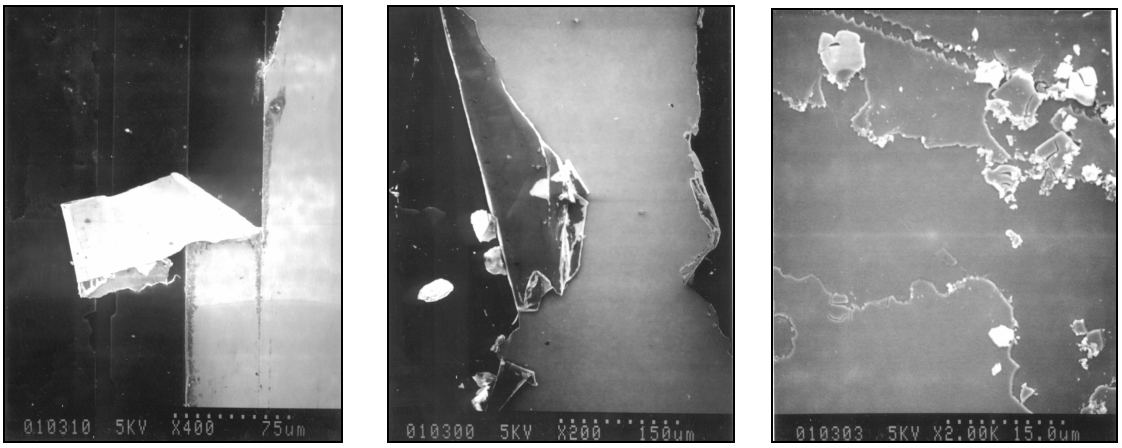

Figure 1.4 Delaminated dielectric capping layers CMP (Zantye, 2005)

1.5 The role of low dielectric constant thin films in integrated circuits

A dielectric material is a substance that is a poor conductor of electricity but is able to hold an electrostatic field. The dielectric constant (k) of a material measures ability of that material to hold an electrostatic field. Ideally the lowest dielectric constant of a material is given a value of 1. As seen in figure 1.5 the device speed is inversely proportional the k value of MLM structure capping layers.

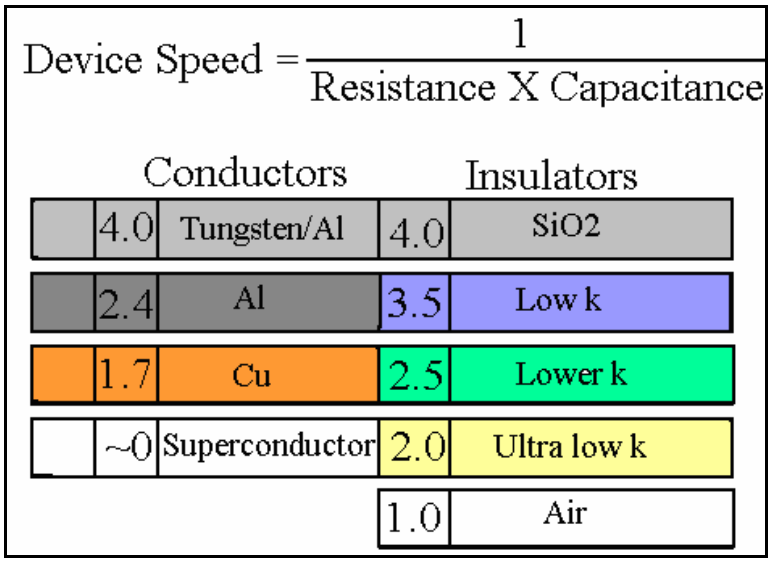

Figure 1.5 IC device speed equation (Bohr, 1995)

Low dielectric constant (low-k) films play a number of roles in the IC (integrated circuits) industry. Their functionality can range from radiation resistance, masking for diffusion, diffusion from doped oxides, protecting of doped films to prevent dopant loss, mechanical or chemical protection, to electronic insulation. Due to its ease of preparation and extensively well characterized properties, the most commonly used dielectric is silicon dioxide (SiO_2) (Zaininger, 1969). Nevertheless the k value of SiO_2 is not low enough to meet the demands of future IC devices. This has prompted the development of alternative low-k materials. The production of alternative low-k materials aim to decrease the dielectric constant value thereby increasing the materials semi-conductive insulation potential. However as materials with lower k values are created, the mechanical properties for these materials began to degrade as shown in figure 1.6.

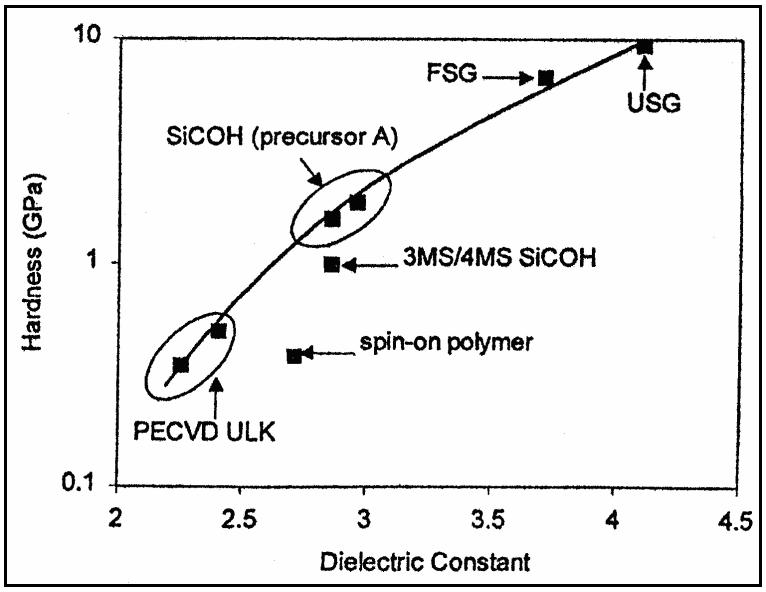

Figure 1.6 Hardness vs. dielectric constant (Ryan, 2005)

To meet industry goals for applications in the monolithic semiconductor technology, the production of new materials with low-k values is urgently needed. As seen in table 1.1 IC device stacking planes, device frequency and plane to plane interconnects are projected to increase through 2010, while the feature size and k values of capping layers in MLM structures are projected to decrease. To meet these MLM structure fabrication goals, capping layers must have good adherence to semi-conductive surfaces and retain good mechanical properties for structural rigidity during device fabrication.

Table 1.1 MLM fabrication projections (Hendricks, 1999)

Year	1996	1999	2002	2005	2010
Feature size (µm)	0.35	0.25	0.18	0.13	0.1
Metal levels	4-5	5	5-6	6-7	7-8
Device frequency (MHz)	200	350	500	750	1000
Interconnect length (meters/chip)	380	840	2100	4100	6300
Dielectric constant (k)	4	2.9	2.3	<2	2~1

1.6 Candidate low-k thin films

In this thesis the adhesion of boro-phosphate–silicate glass (BPSG) and the adhesion of tetraethylorthosilicate (TEOS) to silicon (Si) substrates were evaluated. BPSG low-k films are produced by doping SiO_2 with boron and phosphorous. BPSG is often used as a capping layer because it reduces of sodium contaminates during IC devices fabrication (Walder, 2004). TEOS is used as a low-k material for interconnect technologies because it provides reduced dynamic power dissipation and signal propagation delay (Loke, 1998). Both BPSG and TEOS are deposited by chemical vapor deposition (CVD) process and are known for their smooth topographies as seen in figure 1.7. The BPSG and TEOS low-k films used in this thesis were provided by Syntax Company.

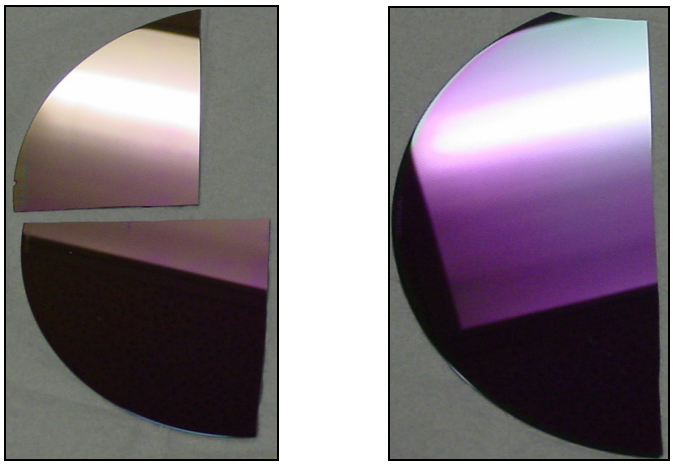

Figure 1.7 BPSG and TEOS low-k wafers, respectively

1.7 Review of adhesion energy for thin films

As previously mentioned, during the fabrication of MLM structures by CMP process many force are induced on the structure. These forces cause interfacial delamination separating the low-k film thins film from the adjacent substrate. The adhesion energy between two materials is can be characterized by the work required to separate the materials from each other. Adhesion energy has also been referred to as interfacial fracture toughness (Zhang, 2004). In order to measure interfacial fracture toughness, the work of adhesion (adhesion energy) as the film is removed from the substrate needs to be analyzed. Traditionally adhesion of thin films has been measured through rudimentary methodologies.

One method of measuring the adhesion of a thin film is the tape test. In the tape test adhesive tape is put on a film surface and is pulled off. The adhesion of the film to the underlying surface is deemed good if the film remains on the substrate. On the other hand, adhesion is deemed bad if the film is removed from the surface while the tape is

ripped away. In addition to tape test, the stud test has been another crude method of measuring adhesion strength. In the stud pull test, the film surface has a stud glued onto it. Adhesion is then measured by the force needed to pull the stud and the film from the underlying substrate. The manner at which these tests measure adhesion often introduce counter productive plastic deformations in the films from the bending, stretching, and tearing associated with the sample preparation. Thus difficulties in interpreting the adhesion results for the tape and stud pull test make them undesirable methods for characterizing or scientifically analyzing adhesion.

1.8 Thesis motivation and objectives

As semiconductor technology moves further into scaled down device structures, measuring the adhesion of low-k thin films to substrates becomes increasingly important. The motivation behind this thesis was to measure the adhesion energy of low-k capping layers by using four point bend (FPB) and nanoscratch testing methods. The objectives of this thesis were to evaluate the material properties of the BPSG and TEOS low-k thin films and optimize the parameters that promote thin film delamination in order to measure the adhesion energy for the FPB and nanoscratch testing methods.

CHAPTER 2: EVALUATION OF MECHANICAL PROPERTIES FOR LOW DIELECTRIC CONSTANT THIN FILMS USING NANOINDENTATION TESTING

2.1 Introduction to nanoindentation testing

The process of indenting can be defined as a method by which a material whose mechanical properties (hardness and elastic modulus) are well known touches another material for which the mechanical properties are unknown or not well defined (Fischer-Cripps, 2002). The method of indentation has origins from the 19th century. In 1822 Moh's hardness scale categorized materials by their ability to leave a permanent scratch on another material. Moh assigned diamond the highest score of 10 on his scale. It was from Moh's method of material hardness characterization that well known methods like the Brinell, Knoop, Vickers, and Rockwell came about. Nanoindentation essentially follows the same principle. However nanoindentation differs from these methods in one important area. While indentation tests like Brinell, Knoop, Vickers, and Rockwell measure the residual impression left on the material with macroscopic tools. In nanoindentation it becomes difficult for measurements to be performed with conventional equipment, due to the small material thicknesses involved. Nanoindentation test results are produced partially by recording the penetration depth of a hard material like the diamond tip (Berkovich tip) illustrated in figure 2.1.

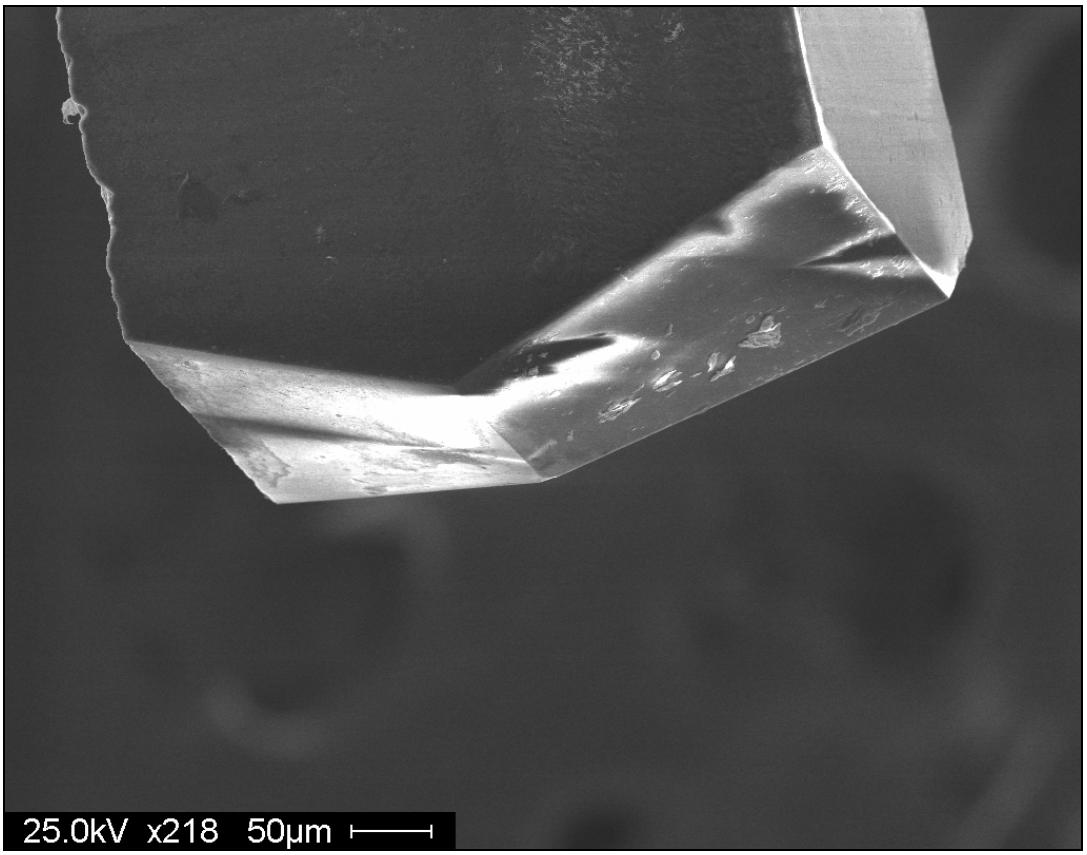

Figure 2.1 SEM of a diamond Berkovich nanoindenter tip

The knowledge of the penetration depth coupled with the known geometry of the indenter provides an indirect measurement of the mechanical properties of the indented material. Nanoindentation testing for thin films has been in development over the past two decades for the purpose of analyzing the physical properties of micron and submicron scale materials. In this thesis the term thin film denotes thicknesses of about 1000 nm - 10 nm. Current nanoindentation systems can position indents within 1 um each other. Newer systems have been integrated with optical systems which enable the user explore the topography of the thin film surface before and after indentations are

performed. Nanoindentation testing is the leading choice for analyzing the hardness and or elastic properties of a material because of its ease in regards to sample preparation.

2.2 Theoretical development of the nanoindentation test

In nanoindentation experiments for the nanometer scale, the indenters are generally made from diamond which can have an axsymmetric or symmetric pyramidal geometry with a very small radius of curvature at the apex. As seen figure 2.2 during a nanoindentation test, the indenter tip is incrementally pushed into the thin film material of interest at a constant speed. The force (P) acting on the tip is measured as the tip is driven into the thin film. Once the tip has reached a specified penetration depth, the tip is then incrementally retracted to its original position above the thin film. From this loading and unloading of the indenter tip the mechanical properties such as hardness and elastic modulus are determined.

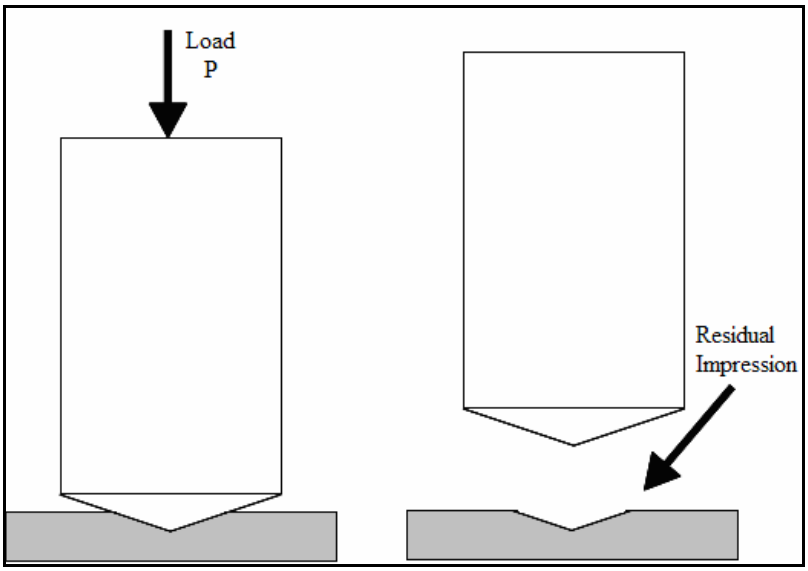

Figure 2.2 Loading and unloading nanoindentation on a material

As the tip is pushed into the material of interest it will plastically deform the material leaving an impression like the ones in depicted in figure 2.3.

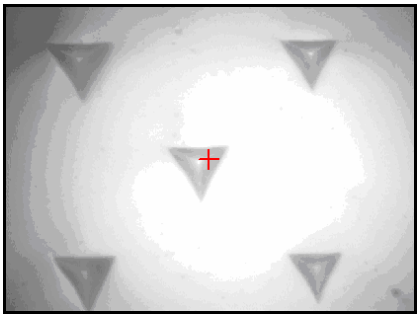

Figure 2.3 40X surface view of fused silica indentation impressions

The load vs. indenter penetration depth curve in figure 2.4 shows the hysteresis between the load and unloading curve that denote the plastic deformation experienced by the indented material.

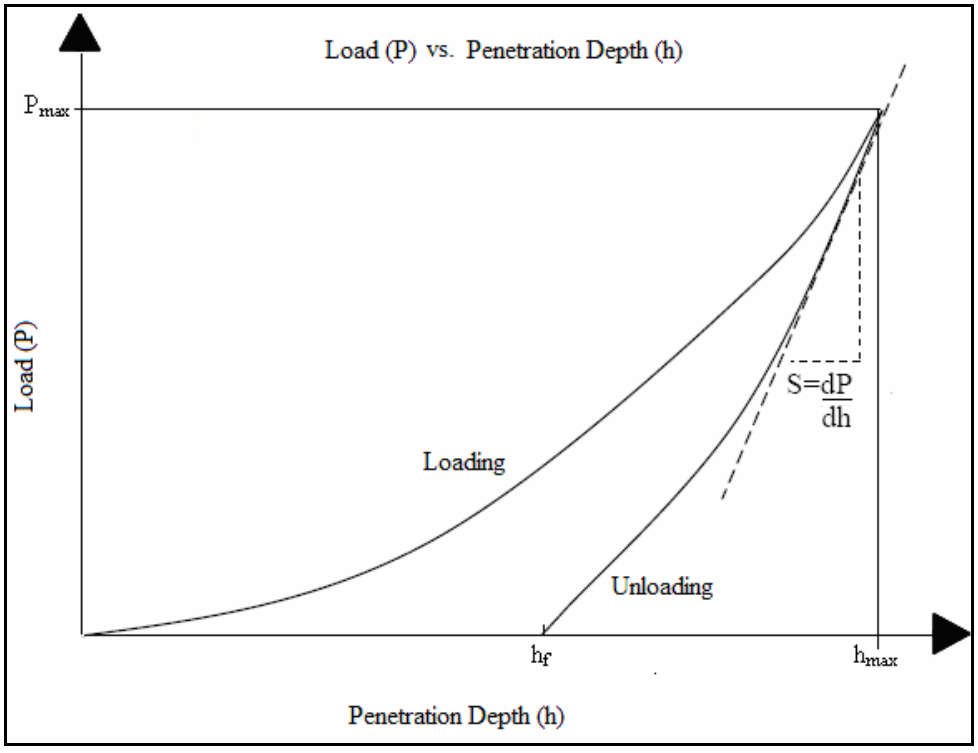

Figure 2.4 Loading and unloading nanoindentation curve (Crawford, 2006)

An important parameter to obtaining the mechanical properties in materials using nanoindentation is the projected contact indenter tip area which varies with the indentation depth. The most agreed upon method for nanoindentation was developed by Oliver and Pharr (Oliver, 1992). The load P from the load vs. depth penetration curve is fitted by parameters B and m in equation 2.1. Equation 2.1 takes into account the resulting depth penetration (h), and final displacement (h_f) after and tip has completely been unloaded from the test sample (MTS, 2001)

$$P = B(h - h_f)^m \tag{2.1}$$

The slope of the unloading curve from the load vs. penetration depth graph is obtained by differentiating equation 2.1 and evaluating it at the maximum penetration depth (MTS, 2001 and Oliver, 1992)

$$S = \frac{Bm(h - h_f)^{m-1}}{h = h_{max}} = \frac{dP}{dh} \tag{2.2}$$

The equation for determining the depth at which the indenter tip is in contact (h_c) with the thin film is

$$h_c = h - \varepsilon\frac{P}{S} \tag{2.3}$$

where ε is a constant which corresponds to the geometry of the indenter being used (Oliver, 1992). For the Berkovich tip ε=0.75 (Fischer-Cripps, 2002). Lastly, with the geometry of the indenter tip known (provided by the manufacture), the projected area A is a function of the contact depth (Oliver, 1992)

$$A = f(h_c) \tag{2.4}$$

The hardness (H) of a material measures the material's resistance to penetration by a hard object (Kalpakjian, 2003)

$$H = \frac{P}{A} \tag{2.5}$$

where P is load applied on the test surface and A is the projected contact area at the load. The thin film elastic modulus (E_f) is determined by the combination of the film modulus and indenter modulus (E_i), called the reduced modulus (E_{rif}) (Oliver, 1992)

$$E_{rif} = \frac{\left(\sqrt{\pi} \bullet S\right)}{2\beta\sqrt{A}} \tag{2.6}$$

where dP/dh is the contact stiffness (S). The geometry correction factor, beta (β) is 1.034 for the commonly used Berkovich indenter (Fischer-Cripps, 2002). The elastic modulus for the thin film is determined using the equation (Oliver, 1992)

$$\frac{1}{E_{rif}} = \frac{\left(1-\nu_f{}^2\right)}{E_f} + \frac{\left(1-\nu_i{}^2\right)}{E_i} \tag{2.7}$$

where ν_f and ν_i are the Poisson ratio of the film and indenter, respectively.

2.3 MTS Nano Indenter® XP

In this thesis the MTS Nano Indenter® XP at USF's advance materials lab was used to indent the BPSG and TEOS low-k thin films for hardness and elastic modulus data. The MTS indenter in figure 2.5 has a maximum applied load of 500 mN, an indenter load resolution of 50 nN, and a displacement resolution of 0.02 nm. The MTS indenter uses Testworks 4 interface software to analyze the collected indentation data.

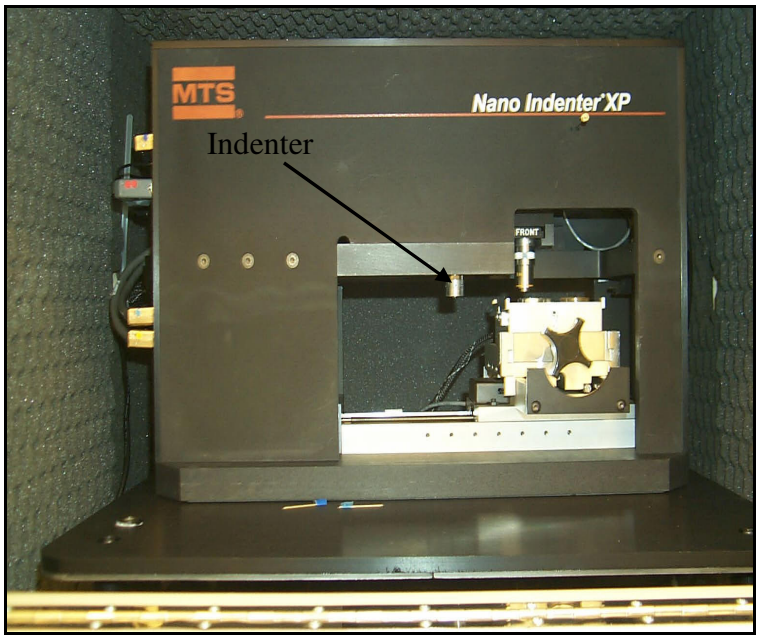

Figure 2.5 MTS Nano Indenter® XP

All indentations done in this thesis used the continuous stiffness measurement (CSM) option. As seen in figure 2.6 the CSM option differs from traditional nanoindentation in that the resultant data is derived from partially unloading the indenter at each load increment and not just at the maximum depth penetration. The advantage of using the CSM option is that it provides viscoelastic behavior of materials which provides information about the storage or loss of the test sample moduli (Li, 2002). The CSM option also provides less sensitivity to thermal drift to allow accurate observation of small volume deformation.

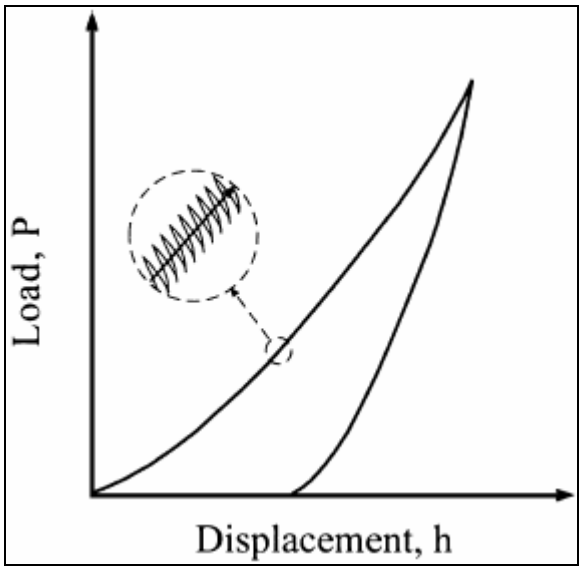

Figure 2.6 Schematic of the CSM loading cycle (Li, 2002)

2.4 Nanoindentation sample preparation

From start to finish sample preparation for nanoindentation test can range from 1 - 10 minutes. First the test sample is mounted on a flattened disk, as seen in figure 2.7. A small amount of adhesive glue (cyanoacrylate also known as Super glue) can be applied between the disk and the bottom of the test sample.

Figure 2.7 Sample mounted on disk

Next the disk is placed on a sample tray like the one depicted in figure 2.8, and then leveled off to insure all the test samples do not exceed a predetermined indenter tip height.

Figure 2.8 Sample tray

Next the sample tray is inserted into the MTS Nano Indenter® XP for material testing as shown in figure 2.9.

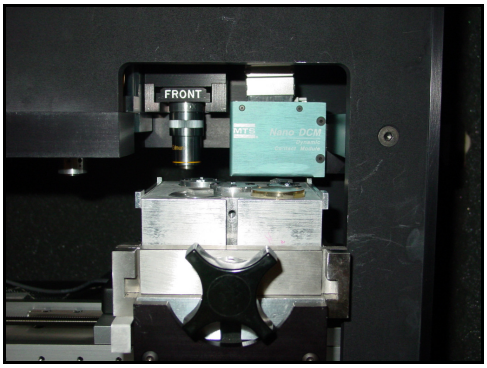

Figure 2.9 Sample tray inserted into MTS Nano Indenter® XP

2.5 Results and discussions of low-k thin film nanoindentation tests

In this thesis the mechanical properties of 9 silicon (Si) wafers with low-k thin films deposited on them were tested using nanoindentation. Although 15 random indents were performed on each low-k thin film, figures 2.10, 2.11 and 2.12 show the profile curves of the BPSG low-k thin film wafer 25, which resembled the modulus, hardness, and load curves profiles for the all thin films tested. Due to insufficient indenter contact area with the low-k thin films, as a rule of thumb the first 20 to 30 nm of the indentations were disregarded (FischerCripps, 2002). This lack of indenter contact area explains the non uniform mechanical properties exhibited at the beginning of figures 2.10 and 2.11.

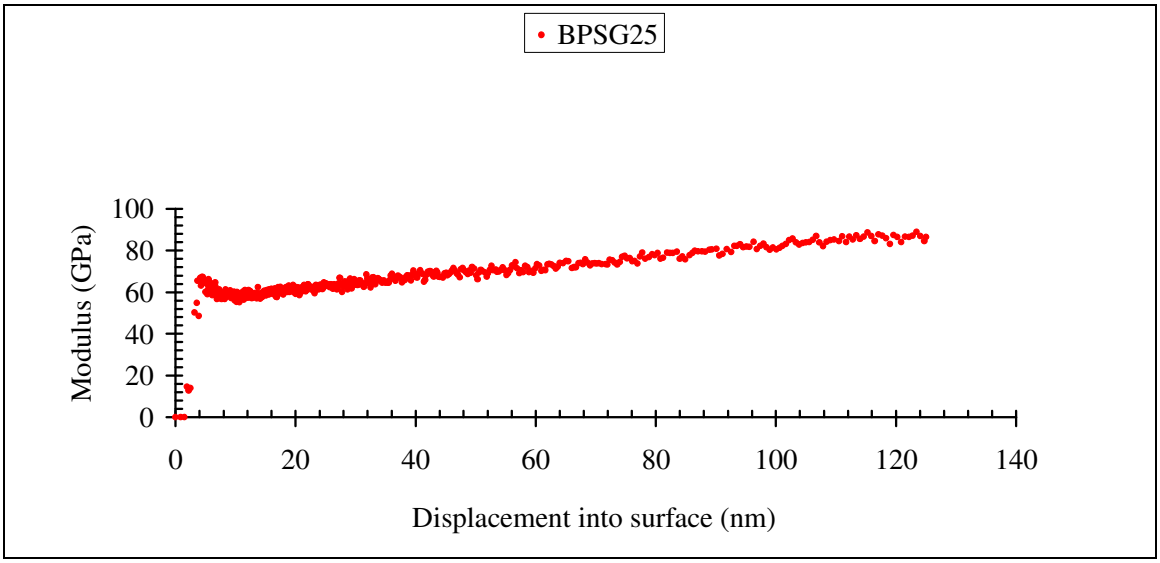

Figure 2.10 BPSG25 sample elastic modulus test

In figure 2.11 the hardness of the BPSG25 film begins to stabilize after 40 nm indenter depth. This steady hardness value indicates that the material is uniform and does not change in material throughout the thickness of the film. In figure 2.12, the plastic deformation that occurred in BPSG25 film can be seen by the difference in the loading

and unloading of the indenter. It can be observed that the BPSG film was plastically deformed to a depth of 80 nm.

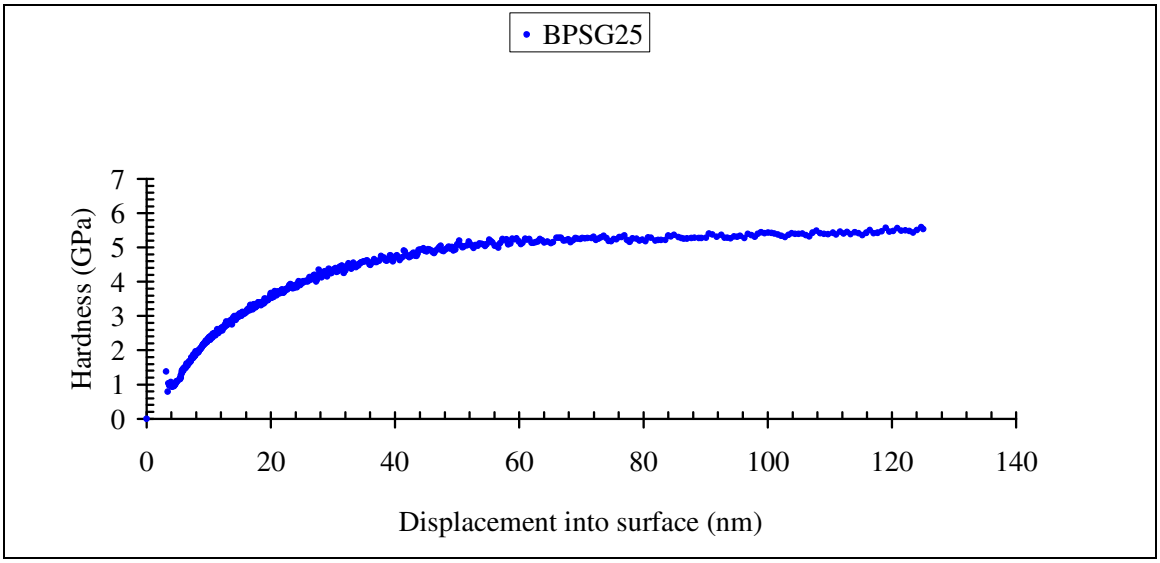

Figure 2.11 BPSG25 sample hardness test

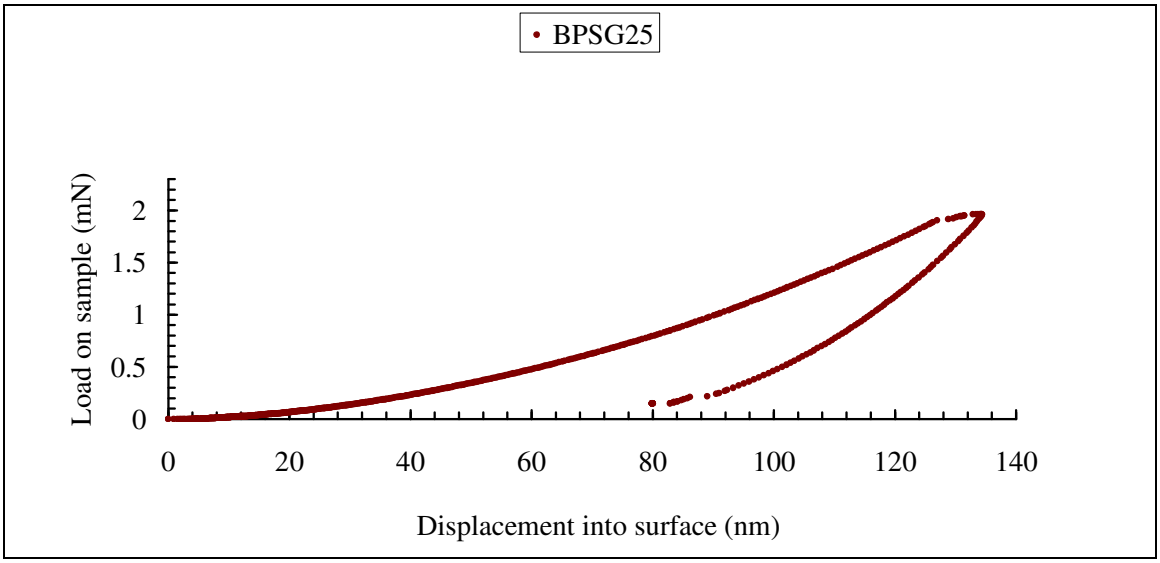

Figure 2.12 BPSG25 sample loading and unloading test

Table 2.1 shows the average value for the mechanical properties of BPSG wafer 1, 21, 22, 23, 24, and 25. The indentation uncertainties for the elastic modulus and hardness of all BPSG and TEOS films were calculated by the Testworks 4 software in the MTS Nano Indenter® XP. Also the BPSG and TEOS mechanical properties were calculated at 10% depth of the thin film thickness to avoid Si substrate effects that may alter the material property values (Oliver, 1992). Table 2.2 shows the average value for the mechanical properties of TEOS wafer 3, 5, 7.

Table 2.1 BPSG low-k material properties

Low-k thin film wafer	Film thickness (nm)	Elastic modulus (GPa)	Hardness (GPa)	Penetration depth (nm)
BPSG1	435	61.300 ± 0.615	4.940 ± 0.192	131
BPSG21	433	64.109 ± 0.859	4.528 ± 0.166	130
BPSG22	430	62.955 ± 0.371	4.734 ± 0.219	129
BPSG23	426	65.045 ± 0.267	4.631 ± 0.490	128
BPSG24	433	63.798 ± 0.429	4.845 ± 0.185	130
BPSG25	623	64.319 ± 0.493	4.327 ± 0.795	130

Table 2.2 TEOS low-k material properties

Low-k thin film	Film thickness (um)	Elastic modulus (GPa)	Hardness (GPa)	Penetration depth (nm)
TEOS3	1.1	82.933 ± 3.373	13.171 ± 0.205	110
TEOS5	1.1	79.198 ± 7.534	13.878 ± 1.372	110
TEOS7	1.1	81.713 ± 5.453	12.021 ± 0.785	110

Depicted in figure 2.13 and figure 2.14 are the modulus and hardness values for both BPSG and TEOS film samples, respectively. These bar graphs show that the mechanical properties of the low-k thin films used in this thesis did not change, and thus were uniform throughout the surface of the wafer.

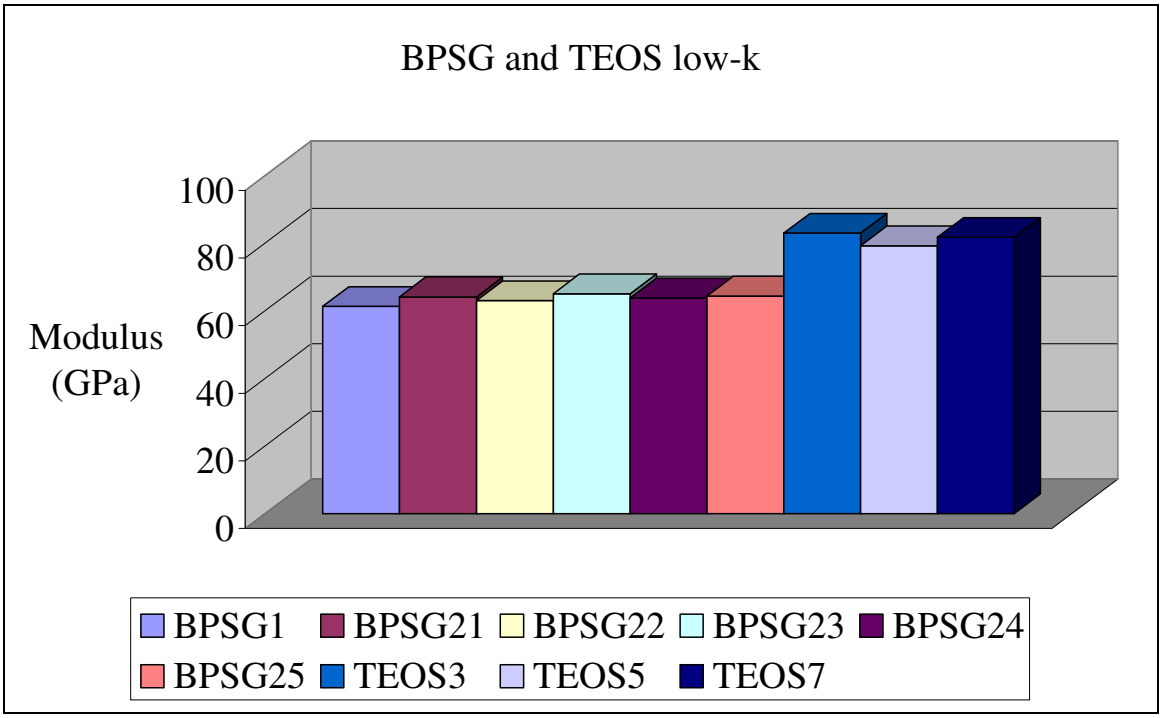

Figure 2.13 BPSG and TEOS modulus values

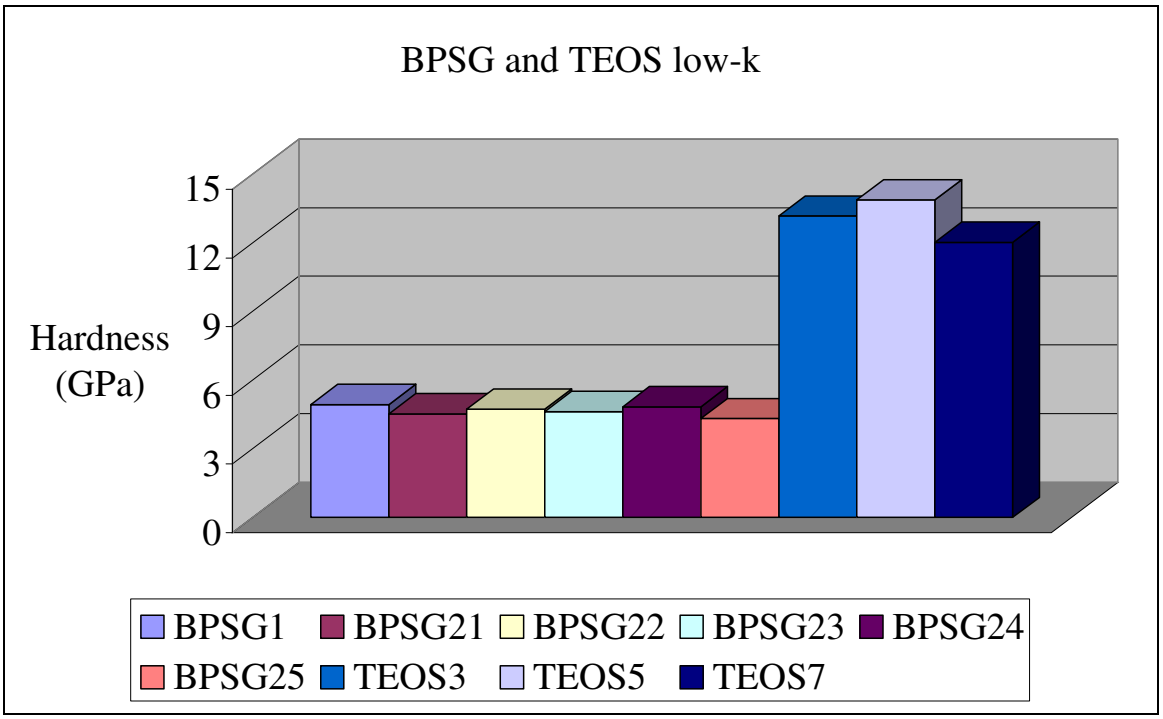

Figure 2.14 BPSG and TEOS hardness values

Before and after performing indentation tests for both the BPSG and TEOS test samples, indentations were also performed on fused silica for indenter tip calibration purposes. The calculation depth of 150 nm was used for calculating the fused silica material properties. Figures 2.15, 2.16, and 2.17 show the modulus, hardness, and load curves of the fused silica sample after all nanoindentation test were completed. Table 2.3 shows that the fused silica properties were within the correct range of 8.5 - 10.5 GPa and 69 - 74 GPa for the hardness and elastic modulus, respectively. The fused silica calibration test also show that since the fused silica properties were correct, the tip was not damaged during the indentations of the BPSG and TEOS films.

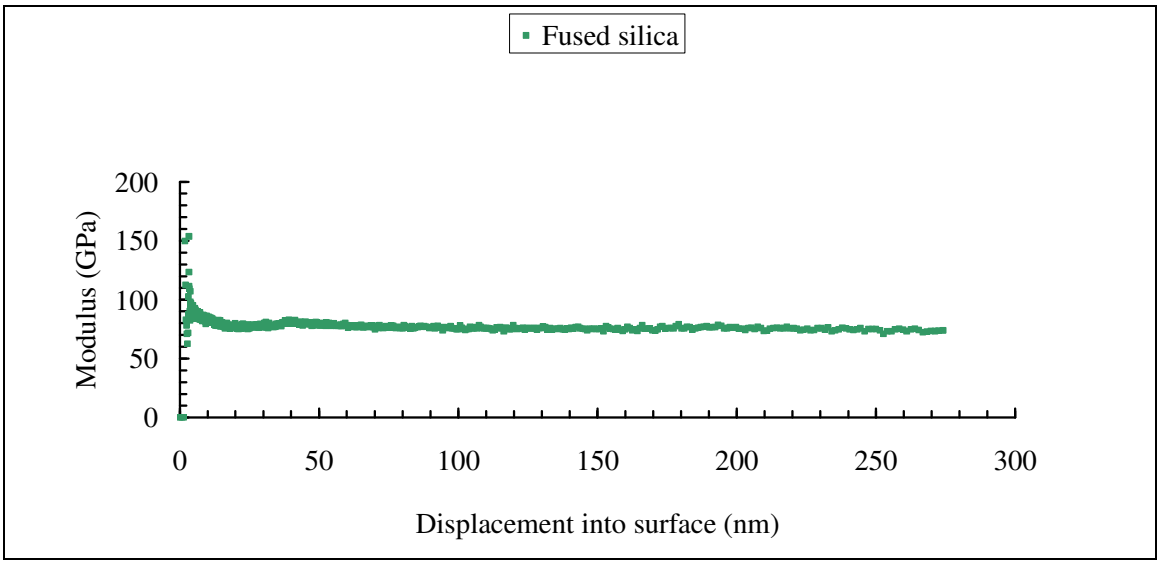

Figure 2.15 Fused silica sample modulus curve

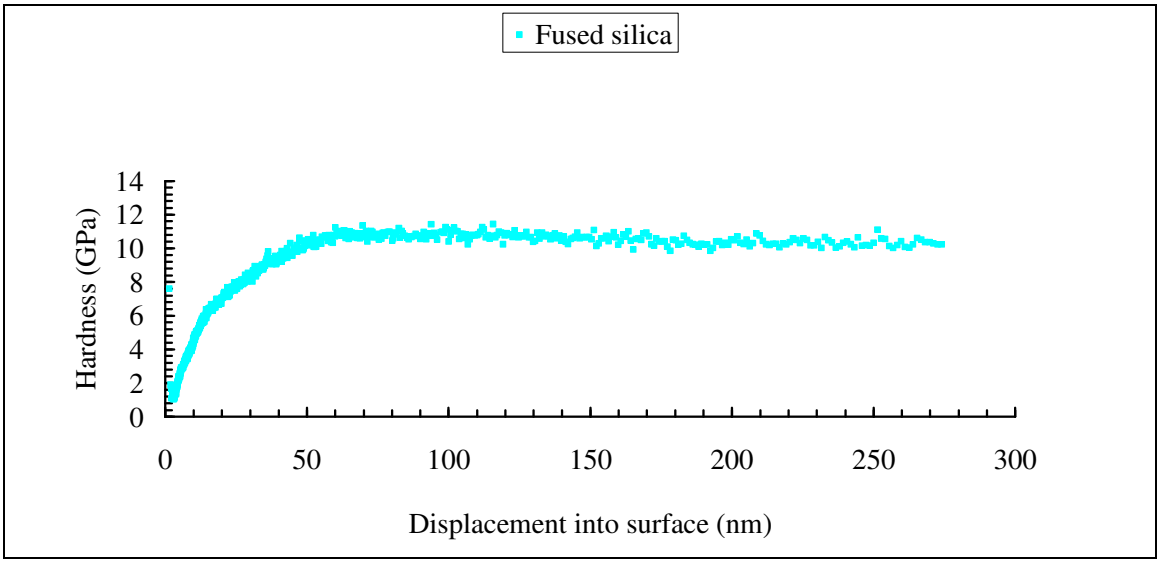

Figure 2.16 Fused silica sample hardness curve

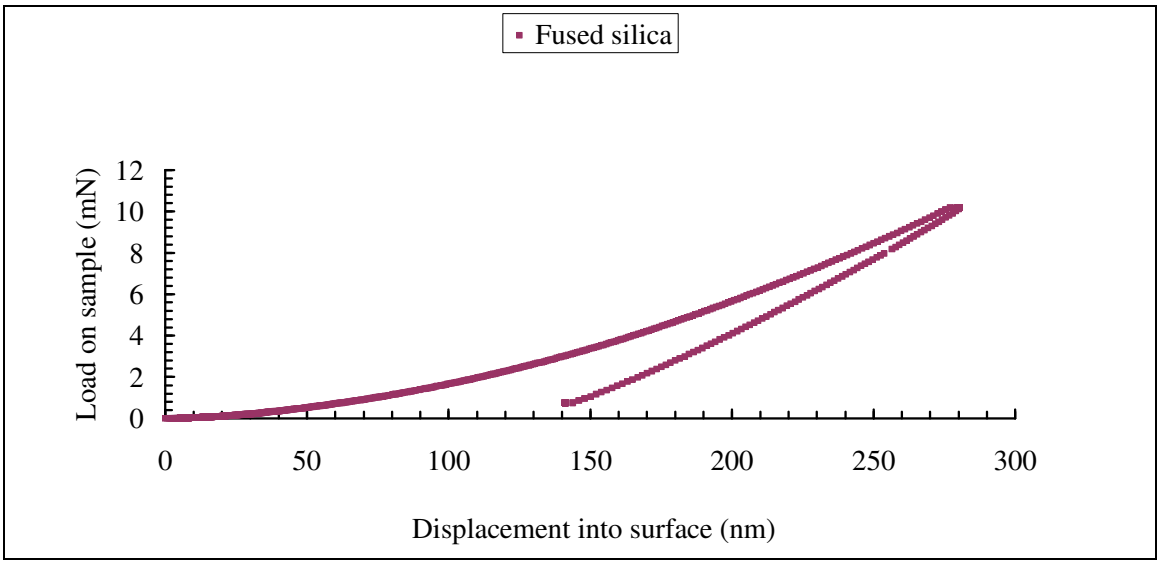

Figure 2.17 Fused silica sample loading and unloading curve

Table 2.3 Fused silica material properties

Fused silica		
Elastic modulus (GPa)	Hardness (GPa)	Penetration depth (nm)
72.016 ± 0.082	10.039 ± 0.665	280

CHAPTER 3: EVALUATION OF ADHESION ENERGY FOR LOW DIELECTRIC CONSTANT THIN FILMS USING FOUR POINT BEND TESTING

3.1 Introduction to four point bend testing

Three point bend and four point bend (FPB) testing has traditionally been used to analysis the fracture toughness of bulk materials. Depicted in figure 3.1 is a ceramic sample that has fractured under an increasing load during a four point bend test.

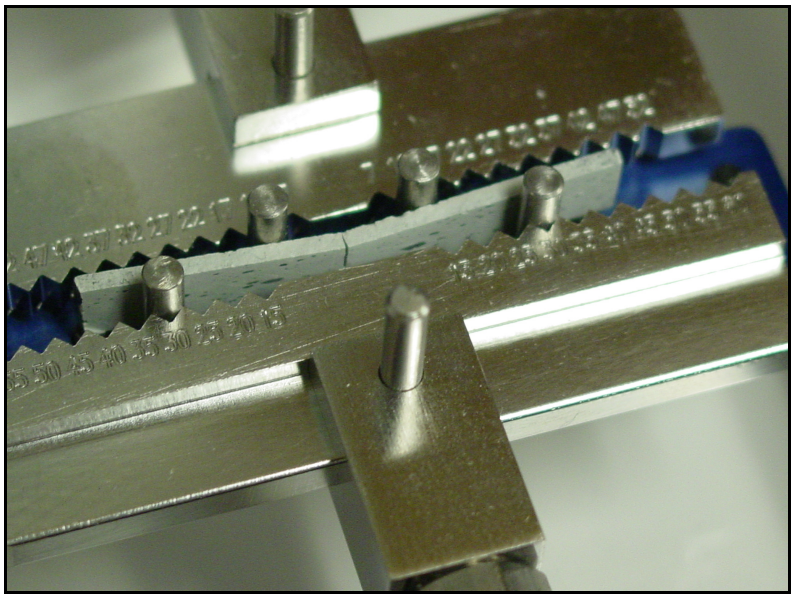

Figure 3.1 Four point bend test on a ceramic sample

The orientation and number of load points differentiate the three point bend from four point bend test. As seen figure 3.2 the three point bend test applies a maximum

bending moment at the center load point of the test sample. However the four point bend load points permit the test sample to experience a maximum bending moment at larger surface area between the inner load pins. This allows defects or weak points that may lead to fracture to be analyzed. The four point bend test has in the past several years been adapted as an alternative method to investigating and measuring thin film adhesion energy.

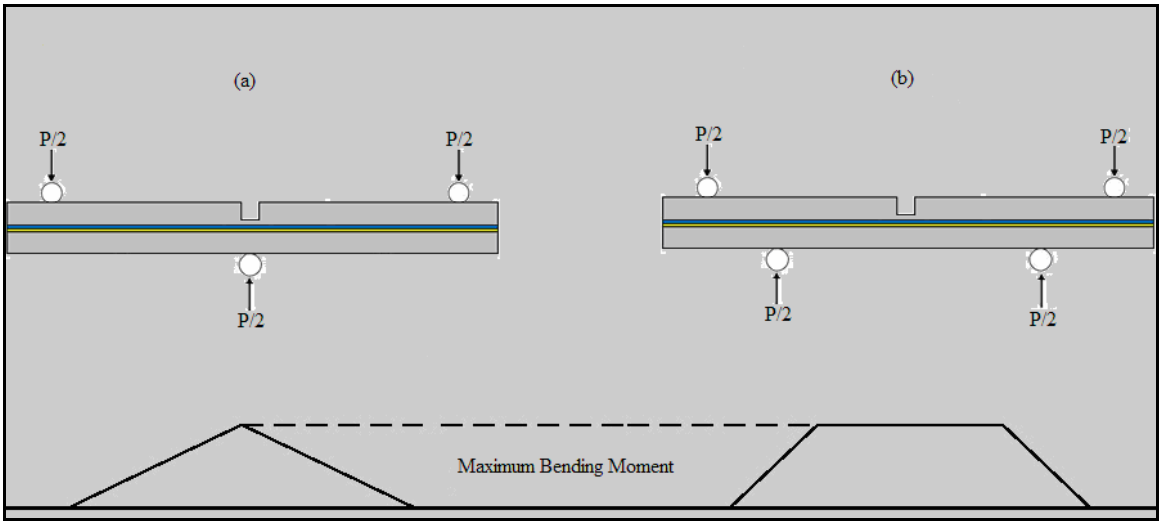

Figure 3.2 Three point bend and four point bend moment diagrams

3.2 Theoretical development for adhesion energy of four point bend testing

In FPB testing, the governing equation for determining the adhesion energy begins with the fundamental concept of internal work. This internal work is often called strain energy (U) (Gere, 2001)

$$U = \int_0^x P\,dx = P \cdot \Delta x \tag{3.1}$$

where P is any value for a force between zero and the maximum value P which corresponds to the elongation of a bar over a distance Δx . In geometric terms, the work

done by the load P is equal to the area under a load vs. displacement curve. The SI unit for strain energy is the joule (J), which is equal to 1 Newton meter (1 J = 1 Nm) (Gere, 2001).

As an actuator presses on the test sample the maximum bending moment occurs in the region between the inner pins. The equation for bending moment in this region is

$$M = PL \tag{3.2}$$

where P equals the force applied on each pin and L is the distance between the outer and inner pin. However the force P from the actuator is divided equally between the two pins on either side of the sample being tested. Thus P=P/2 at each of the pin positions making equation 3.2 become

$$M = \frac{PL}{2} \tag{3.3}$$

The angle of rotation of a beam axis is θ

$$\theta = \frac{ML}{E_{rfs} I_S} \tag{3.4}$$

where θ is defined as the angle of the arc length that the test sample produces while being bent by the actuator load (Gere, 2001).

E_{rfs} is the reduced elastic modulus for the test sample (Ugural, 2003)

$$\frac{1}{E_{rfs}} = \frac{\left(1-\nu_F{}^2\right)}{E_F} + \frac{\left(1-\nu_S{}^2\right)}{E_S} \tag{3.5}$$

where E_f is the thin film modulus, E_s is the substrate modulus, ν_F is the Poisson ratio of the thin film, and ν_S is the Poisson ratio of the substrate. In this thesis it is assumed that since there is such a great disparity in thickness between the substrate

(approximately 1.45×10^{-3} m) and the thin film (approximately 425×10^{-9} m), the effect of low-k film on the test sample bending is negligible. Thus the material properties of the thin film in regards to the reduced modulus are assumed zero, and the reduced modulus of the FPB test sample is now

$$\frac{1}{E_{rfs}} = \frac{\left(1-\nu_S{}^2\right)}{E_S} \tag{3.6}$$

The moment of inertia (I_S) for the FPB test sample is

$$I_S = \frac{B\,H^3}{12} \tag{3.7}$$

where B is the width of the test sample and H=H1+H2 is the height of the total thickness of the test sample Si substrate as seen in figure 3.3 (Gere, 2001).

Combining the angle of rotation of a beam axis (equation 3.4) and bending moment (equation 3.3) on the sample we obtain the equation for strain energy of the test sample (Ugural, 2003)

$$U = \frac{M\theta}{2} = \frac{3P^2L^3}{2E_{rfs}BH^3} \tag{3.8}$$

To obtain the equation for adhesion energy, the reduced modulus (equation 3.6) is applied to the strain energy (equation 3.8). The strain energy is then divided by area of the width (B) and length (L) of the sample. The equation for the adhesion energy of the interfacial delamination is then

$$G = (C)\frac{3\left(1-\nu^2\right)P^2{}_cL^2}{2E_SB^2H^3} \tag{3.9}$$

where P_c is the critical load or load at the plateau region when delamination occurs, C is a non dimensional parameter for the substrate height and material properties (Zhenghao,

2005). Since the top and bottom substrate height and materials properties are the same, C=42/48. The final equation for adhesion energy with SI units of (J/m^2) is (DTS, 2004)

$$G = \frac{21(1-\nu^2)P^2{}_cL^2}{16E_sB^2H^3} \tag{3.10}$$

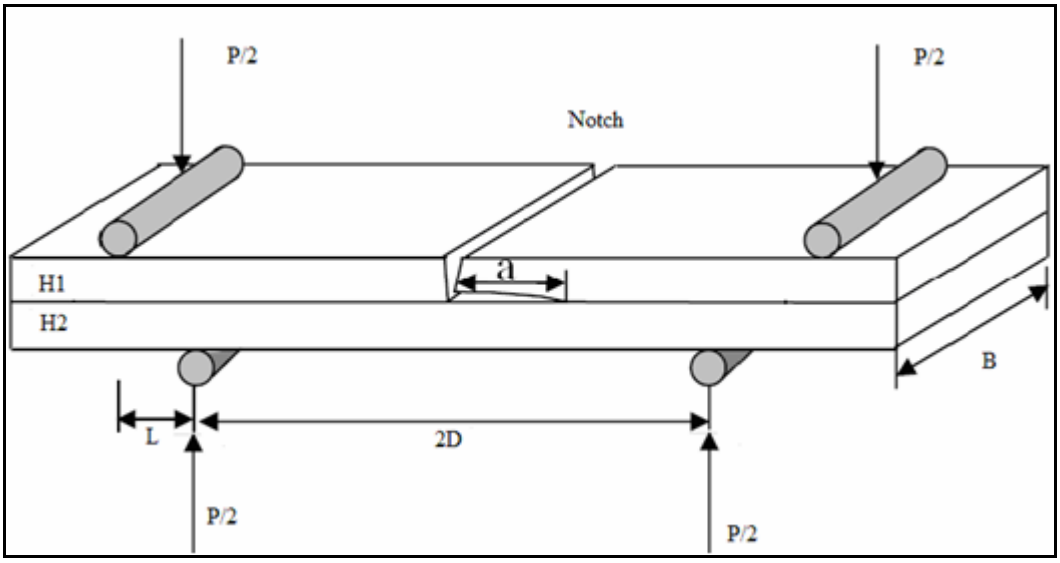

Figure 3.3 A schematic of a FPB sample (Zhenyu, 2005)

3.3 DTS Delaminator test system

In this thesis the DTS Delaminator test system at USF's advance materials lab was used to evaluate the BPSG and TEOS low-k film adhesion energy. As seen in figure 3.4 the system is comprised of three main components: the computer system with DTS Delaminator software, the four point delaminator tester, and data acquisition box.

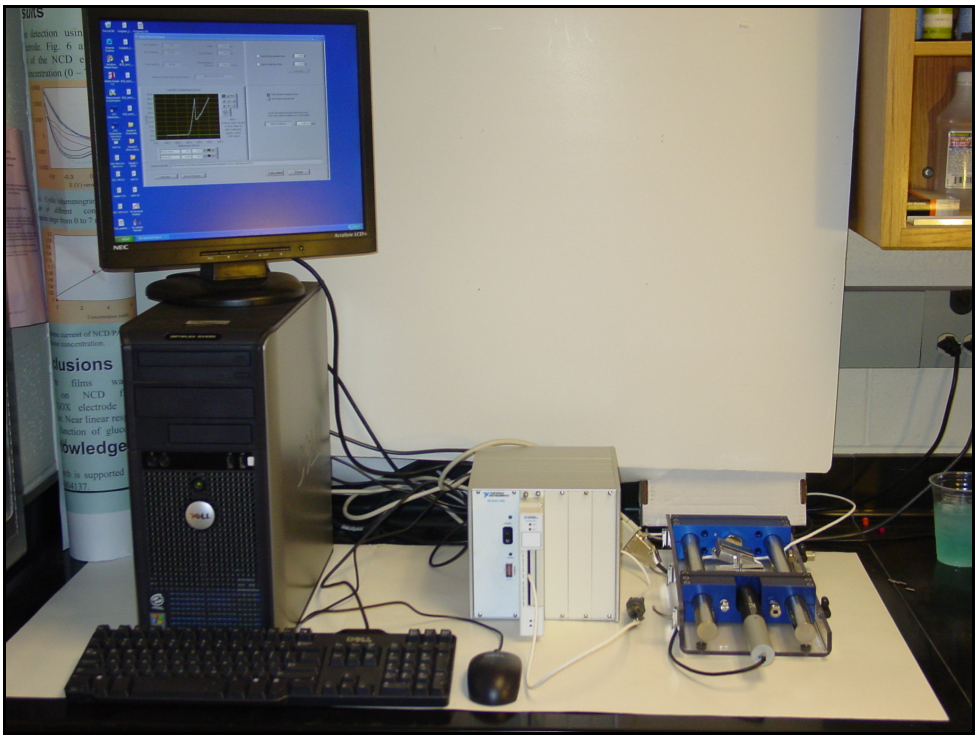

Figure 3.4 DTS Delaminator test system

The four point delaminator tester is sustainable for stability because it is encompassed around a mechanically stiff frame. The system provides ultra-high resolution for the linear actuator with a range of 50 mm with sub-micron resolution (DTS, 2004). The ultra-high resolution allows the actuator to be able to control increment motion as small as 50 nm. The load cell featured in figure 3.5 is built for maximum load of 180 N. The system is also rated for a temperature range of -20 - 85 degrees centigrade (DTS, 2004).

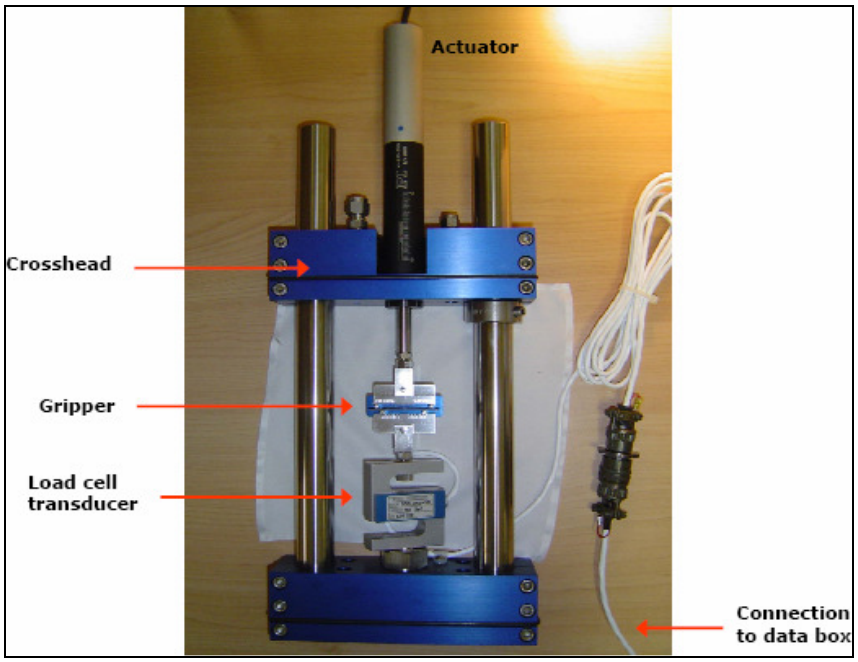

Figure 3.5 DTS Delaminator test system frame (DTS, 2004)

3.4 FPB sample preparation

FPB test sample preparation can range from 1 day to 1 week. First two square wafers are scribed into 50 mm X 50 mm pieces. As seen in figure 3.6 one wafer is a blank silicon (Si) wafer and the other wafer contains the target film (TEOS or BPSG).

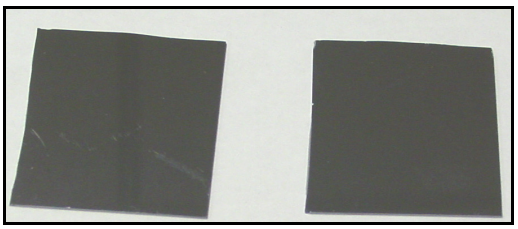

Figure 3.6 50 mm X 50 mm diced silicon sample (left) and low-k sample (right)

3.5 FPB wafer bonding

For bonding the two squares EPO-Tek 375 epoxy is prepared using the resin and harder in figure 3.7. The epoxy mix is composed of a 10:1 ratio of resin and hardener, respectively.

Figure 3.7 EPO-Tek 375 resin (left) and hardener (right)

After the epoxy is prepared, it is then applied to the surface of wafer not containing the film of interest using a razor tip. However, as seen in figure 3.8 this method of applying epoxy results in a non uniform coating with a thickness over 1 um.

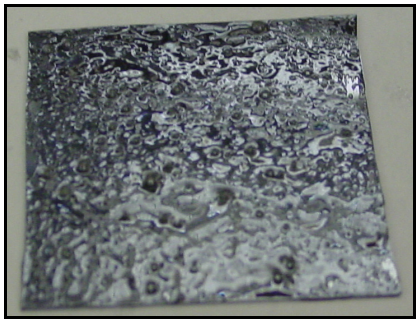

Figure 3.8 EPO-Tek 375 epoxy applied on Si wafer using a razor tip

A different method of applying the epoxy mix on the Si wafer is illustrated in figure 3.9. Figure 3.10 shows the uniform layer that can be put on the silicon wafer by using a disposable pipette nozzle to apply the epoxy.

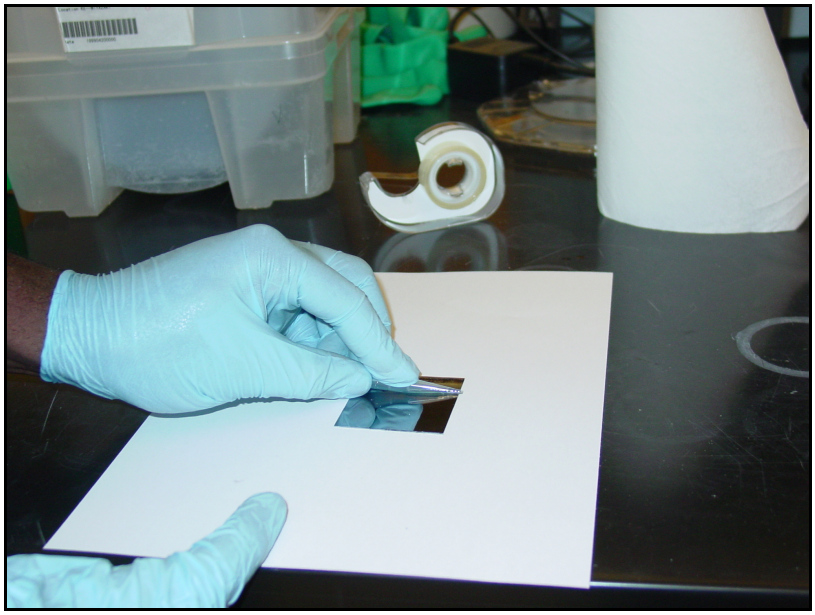

Figure 3.9 EPO-Tek 375 epoxy applied on Si wafer using a pipette nozzle

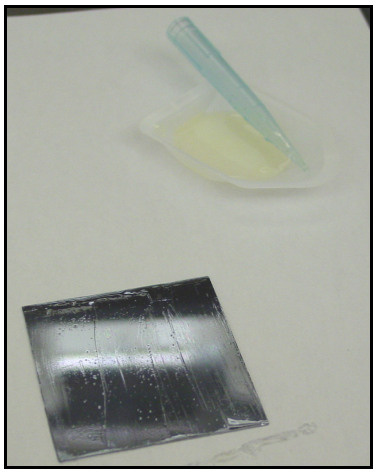

Figure 3.10 EPO-Tek 375 epoxy on Si wafer

The silicon wafer with the target film (BPSG or TEOS) is then sandwiched together with the blank Si wafer coated with the epoxy. To remove any air between the FPB sample the pressing set up seen in figure 3.11 is used to apply a distributed force on the sample. Figure 3.12 and 3.13 shows how the two paper clamps are used to sandwich the samples to minimize the epoxy thickness and remove any trapped air between the FPB samples.

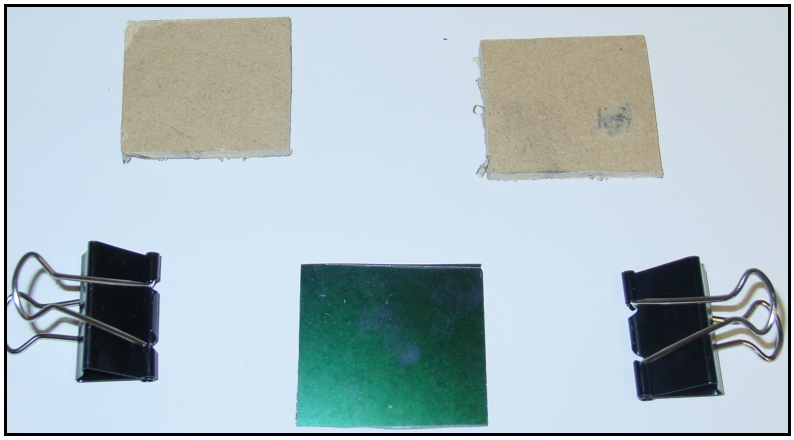

Figure 3.11 FPB sample clamping setup

Figure 3.12 FPB sample clamping

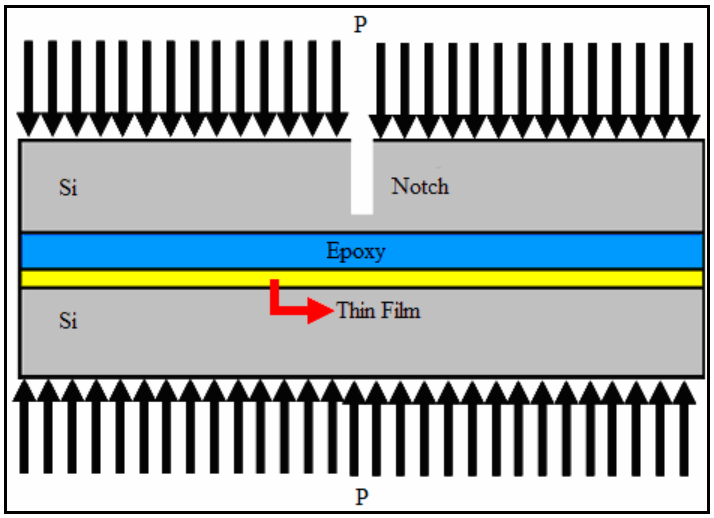

Figure 3.13 Schematic of FPB sample clamping

Nevertheless, using paper clamps was found to be ineffective in reducing the epoxy thickness and removing trapped air between the FPB samples.

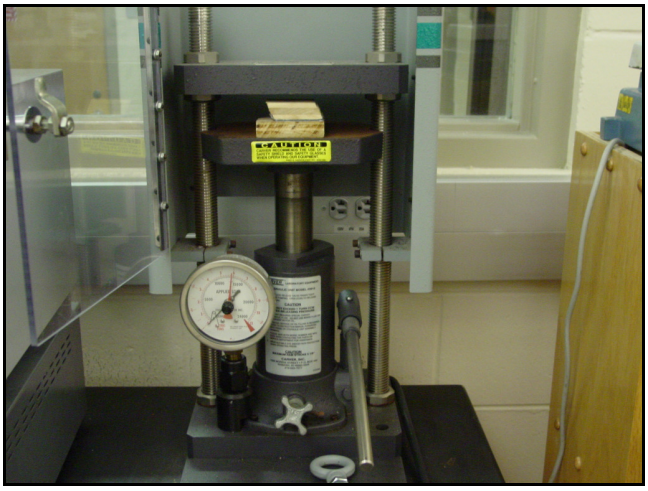

Figure 3.14 FPB sample hydraulic clamping setup

Seen in figure 3.15 is a new pressing method that was implemented. This method involves placing the test sample between two wooden blocks then applying pressure on the blocks with a hydraulic press.

Figure 3.15 FPB sample hydraulic clamping with wooden blocks

3.6 FPB wafer epoxy curing

To cure the epoxy in the samples, the FPB sample are placed in a furnace and heated to 100 degrees centigrade for 1 hour. Figure 3.16 shows the Lindberg/Blue tube furnace used to cure the epoxy in the samples.

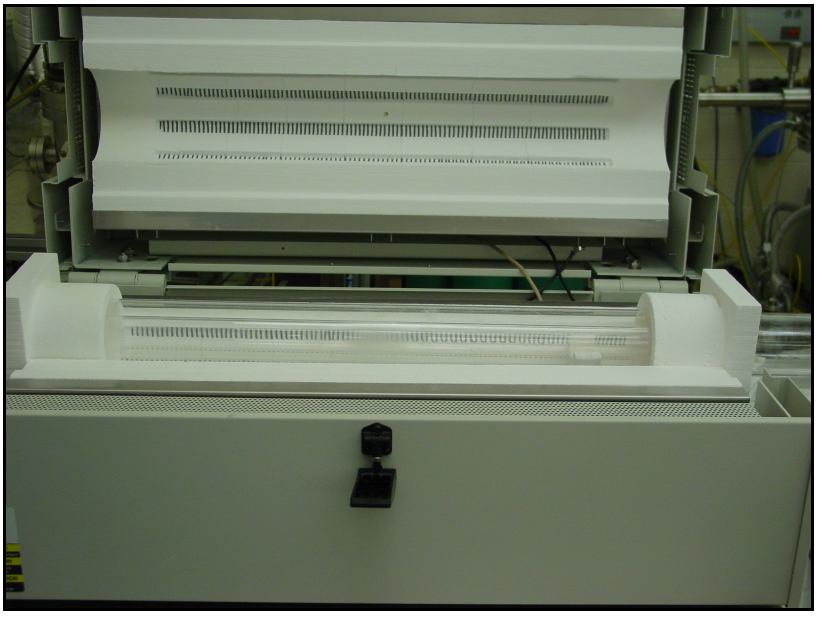

Figure 3.16 Lindberg/Blue tube furnace

The disadvantage with curing FPB samples with the Lindberg/Blue tube furnace is that the cool down time takes 5 hours and only 1 sample could be placed in the furnace at a time when using the Lindberg/Blue furnace. The Lindberg/Blue tube furnace was replaced with the Thermolyne 4800 furnace in figure 3.17, which allowed multiple samples to be cured simultaneously. However, the cool down time when using this furnace was 3 hours.

Figure 3.17 Thermolyne 4800 furnace

3.7 FPB sample wafer dicing

After the curing process is complete the test sample is then diced into 50 mm X 7 mm rectangular samples using the MA 1006 Dicing Saw at USF's Nanomaterials & Nanomanufacturing Research Center (NNRC). Each test sample prior to dicing is placed on a protective blue tape which holds the sample steady while dicing is performed.

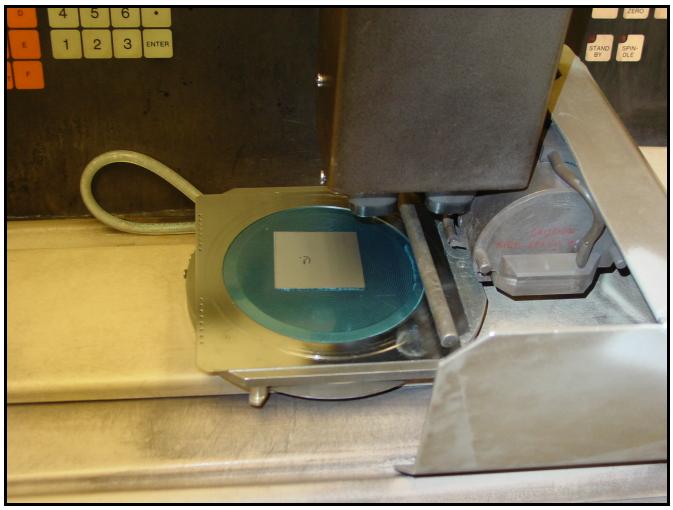

Figure 3.18 MA 1006 Dicing Saw available at the NNRC

3.8 Notching of the FPB sample

To assist in inducing an interfacial delamination, a notch is cut at 85% of the thickness of the blank Si wafer (top substrate) using a 100 um diamond resin blade saw. This notch is illustrated in figures 3.19 and 3.20. In this thesis the thickness of the Si wafers used was 0.74 mm.

Figure 3.19 Diced and notched FPB sample

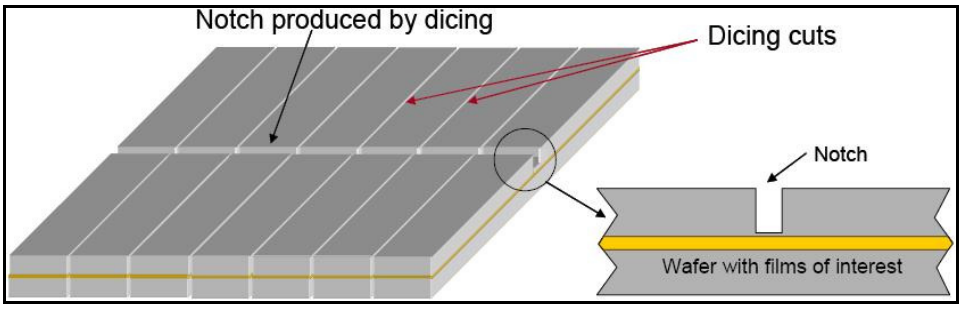

Figure 3.20 Notch cut (DTS, 2004)

3.9 FPB testing using the DTS Delaminator test system

Illustrated in figure 3.21 is the orientation of the FPB test sample before FPB testing begins. As seen in this figure, the two outer metal dowel pins are placed at the 35 mm markers facing the notched side of the test sample. The test sample is then placed on the set screws to reduce any frictional affects that could lead to reduced accuracy of the adhesion measurement. Next, the two inner dowel pins are placed on the non notched side of the test sample at the 27mm markers.

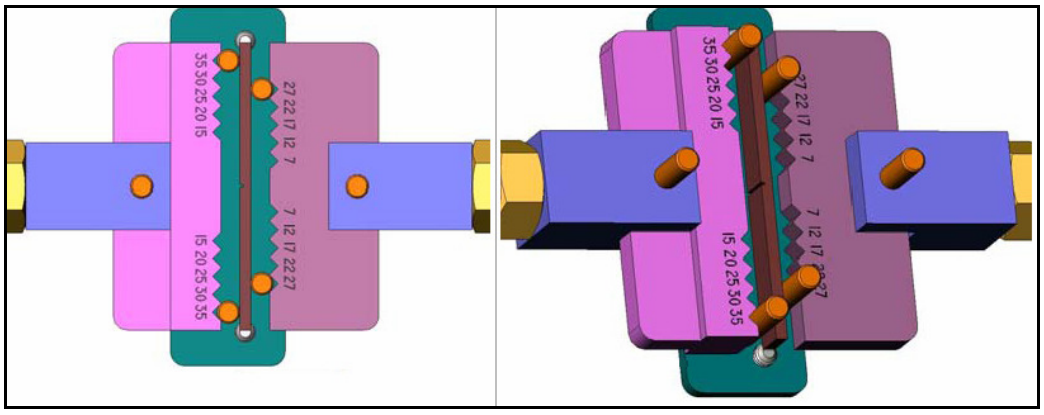

Figure 3.21 FPB sample set up (DTS, 2004)

3.10 FPB sample preload and loading test

Before the four point bend test begins, a preload of 0.1 N is applied onto the sample by the actuator to ensure that the sample is securely in contact with the load pins. Once the preload force is reached, the actuator then begins to displace at a specified constant velocity to start the FPB test. The shaded pink region in figure 3.22 shows that the force experienced by the sample increases linearly as the actuator displacement increases. The figure 3.22 also illustrates that the notch cut in the FPB sample is unaffected during this point of the delamination test.

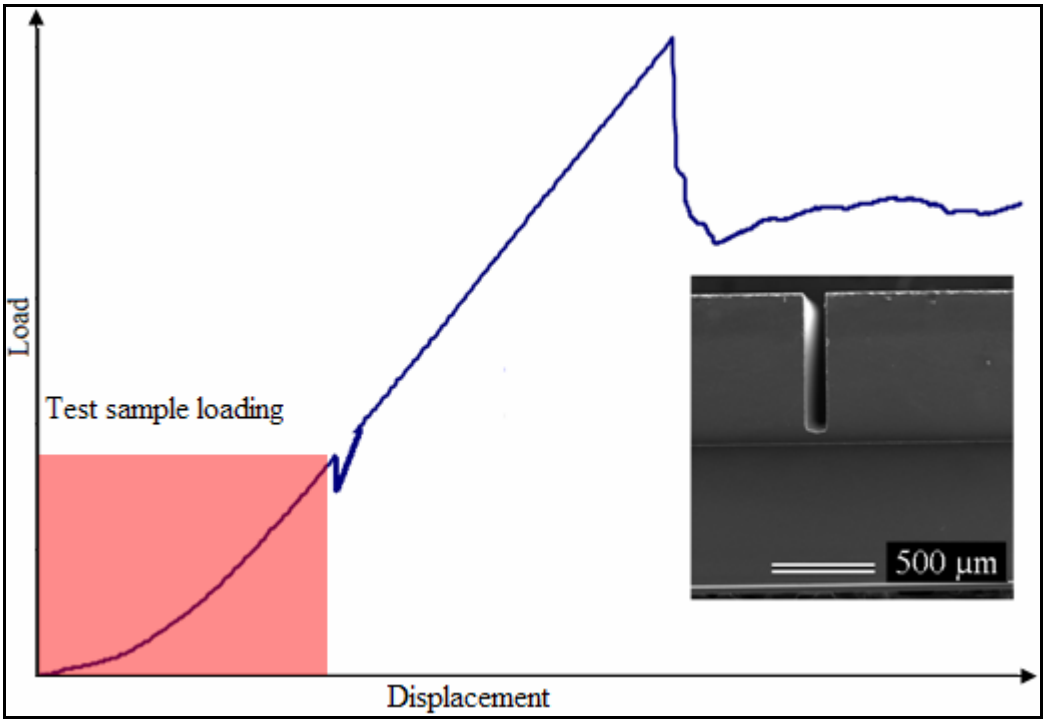

Figure 3.22 FPB sample loading

3.11 Notch crack propagation

As the sample is continually loaded a notch crack begins to emerge from the notch cut and propagates downward towards the interfacial surface where it arrests (Zhenyu, 2005). The small abrupt load drop in the pink shaded region in figure 3.23 marks the strain release in the sample from the notch crack.

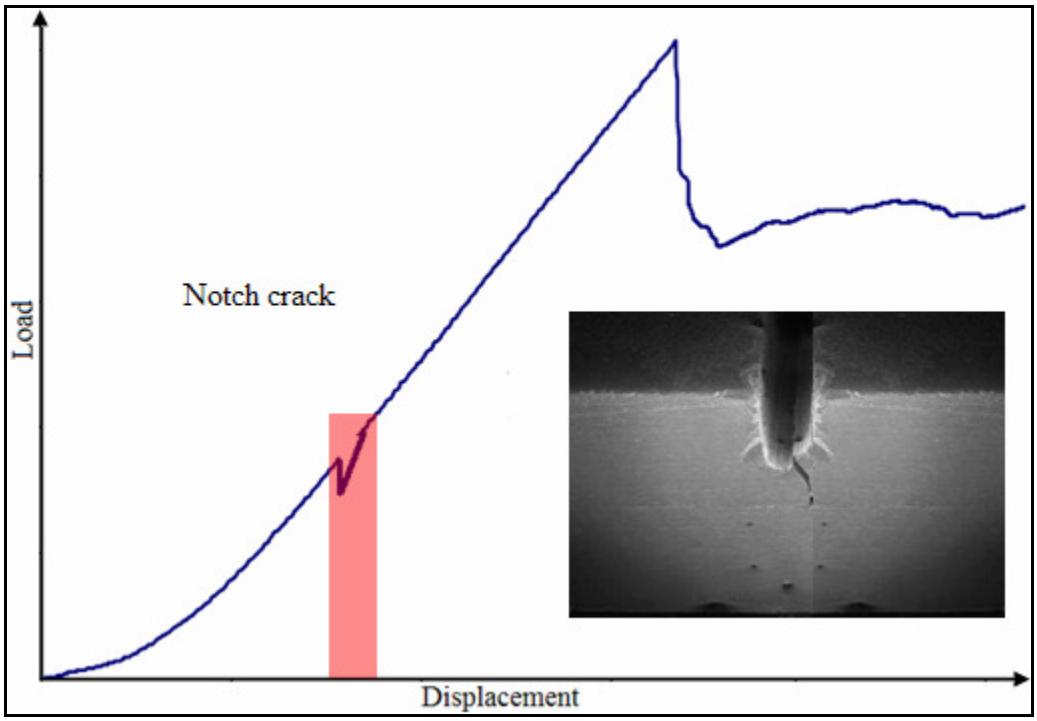

Figure 3.23 FPB sample notch crack

3.12 Interfacial delamination

Once the notch crack is achieved, strain energy in the sample continues to build until a critical load is reached. As seen in the pink shaded region in figure 3.24, the abrupt load drop marks where interfacial delamination in the FPB sample begins. The interfacial delamination then begins to propagate horizontally along the interfacial layer from the arrested notch crack location. As the delamination propagates, the required

force needed to maintain delamination remains unchanged. This plateau region of constant load is used to obtain adhesion energy of thin films.

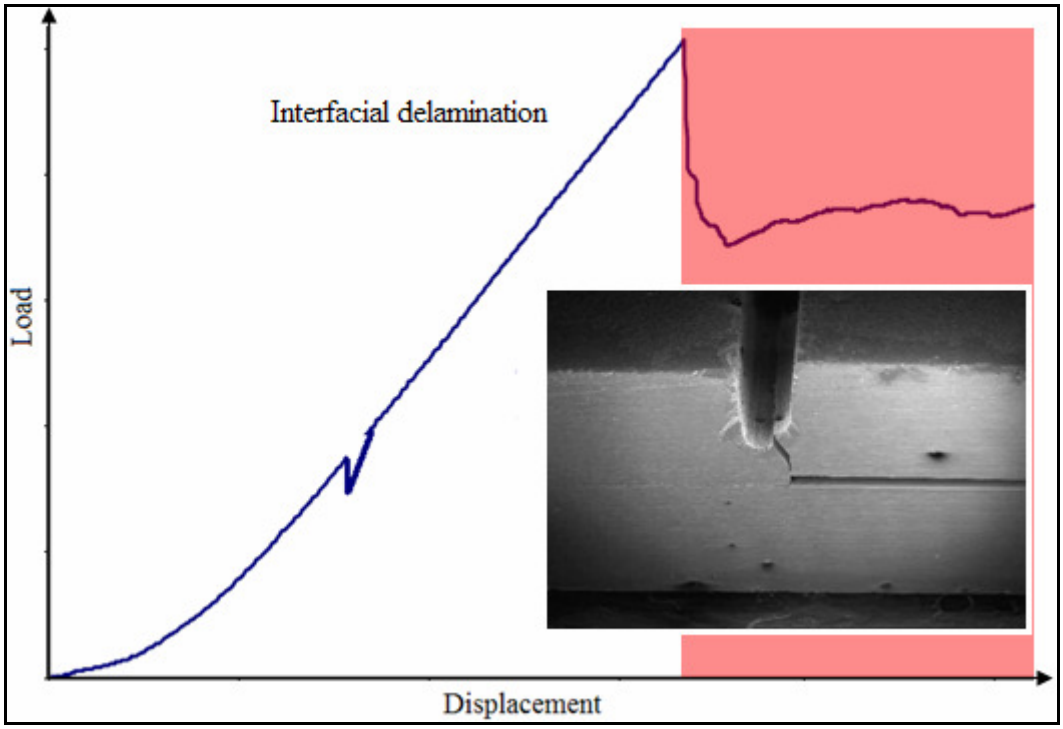

Figure 3.24 Interfacial delamination

3.13 Results and discussions of adhesion energy using four point bend tests

The parameters for the FPB test were optimized to improve delamination in the FPB samples. Initially notch cuts on the FPB samples were cut to 75% - 50% of the thickness of the top Si wafer. Figure 3.25 shows load vs. actuator displacement profile of FPB samples that had the notch cut less than 85% of the top Si wafer. It was observed that all of the samples that had notches cut less 85 % of top Si wafer did not delaminate. It was also observed that the propagation of the notch crack to the interfacial surface did not occur in any of these samples. Figure 3.25 also illustrates that these samples fractured without delaminating because the shallow notch cuts allowed too much strain

energy build up in the sample. In this thesis all FPB sample notch cuts were cut at 85% depth of the top Si wafer. This notch cut criterion proved to be a very crucial parameter in achieving delamination in the samples.

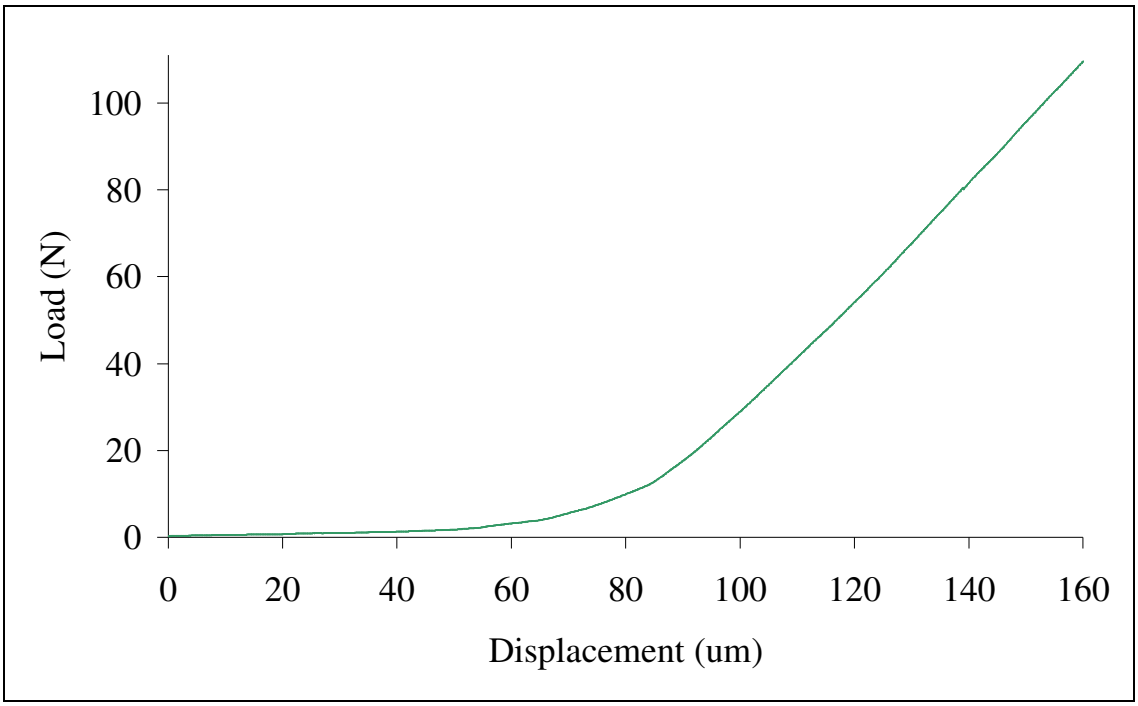

Figure 3.25 Load vs. displacement curve for notch depth below 85%

Figure 3.26 shows load vs. actuator displacement profile of FPB samples that experienced an actuator displacement speed greater than 1.5 um/s. It was observed that the strain energy in the samples built up too quickly causing the sample to fracture prematurely with no notch crack propagation. In this thesis the FPB actuator displacement speed press of 0.8 um/sec - 1 um/sec was used successfully achieve delamination in both the TEOS and BPSG samples.

The load vs. actuator curve in figure 3.26 also resembles the load vs. actuator profile of FPB samples when the inner metal dowel pin spacing was less than 27 mm

apart. It was observed that a larger bending moment was applied to the FPB sample during the actuator displacement. This large bending moment rapidly applied strain in the sample causing the sample to fracture prematurely with no notch crack propagation. In this thesis the inner and outer metal dowel pin spacing for all FPB tests were 27 mm and 35 mm, respectively.

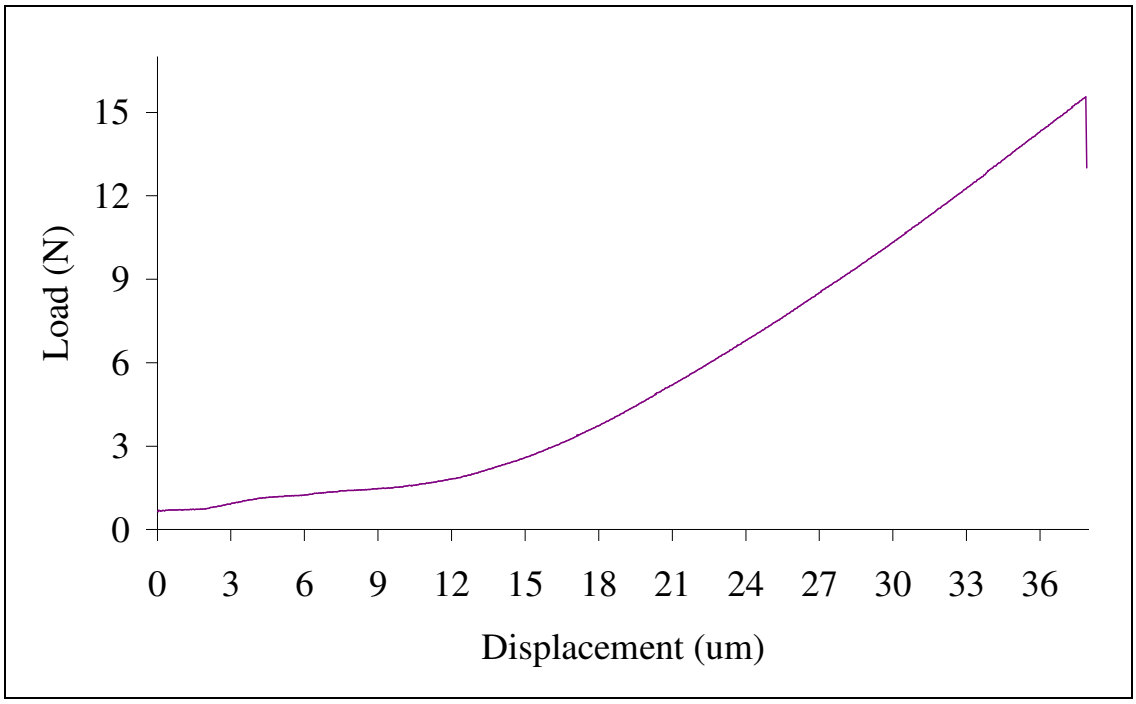

Figure 3.26 Load vs. displacement curve (actuator speed greater than 2 um/sec)

Figure 3.26 shows the load vs. actuator curve profile for FPB samples when the actuator displacement speed was slowed below 0.7 um/s once a notch crack occurred. However this reduction in actuator pressing caused the sample to fracture near the load cell maximum value of 180 N. This phenomenon is a result of the actuator displacement lagging behind the interfacial delamination which prevented interfacial delamination at a steady load.

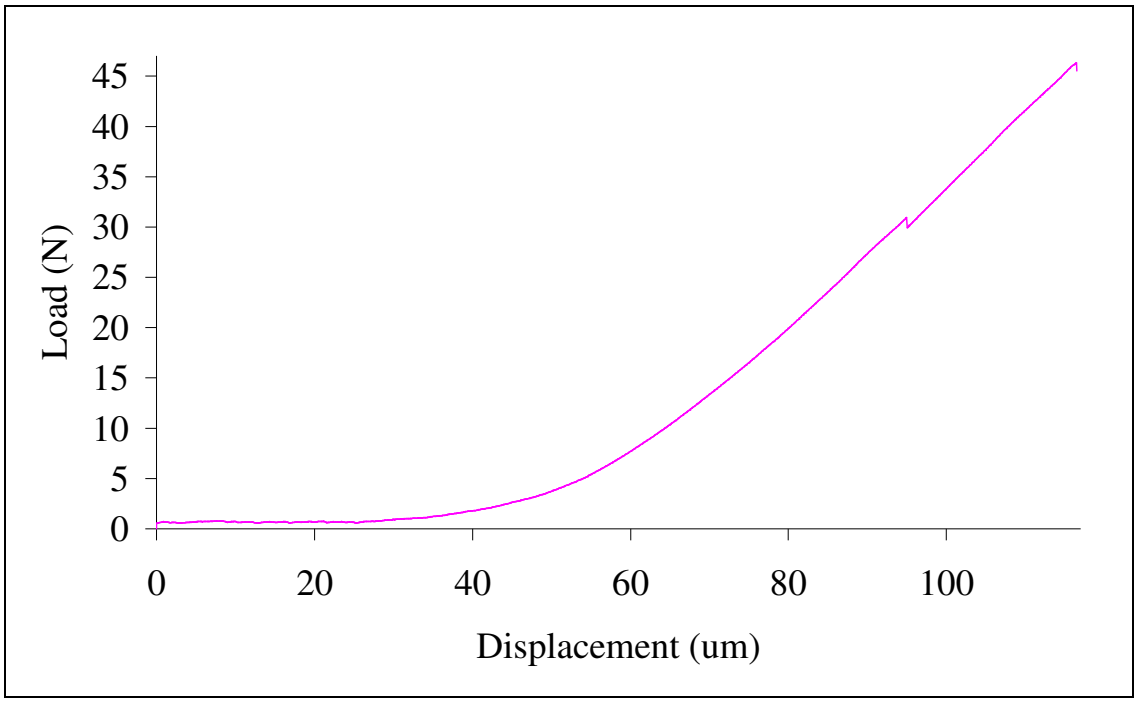

Figure 3.27 Load vs. displacement curve (actuator speed decreased after notch crack)

Figure 3.28 shows the load vs. actuator curve profile of partially delaminated FPB samples. It was observed that partial delamination like the ones depicted in figures 3.29 and 3.30 resulted from a combination of applying a non uniform thick epoxy layer greater than 1 um and insufficient sample clamping pressure to remove trapped air during the FPB sample preparation.

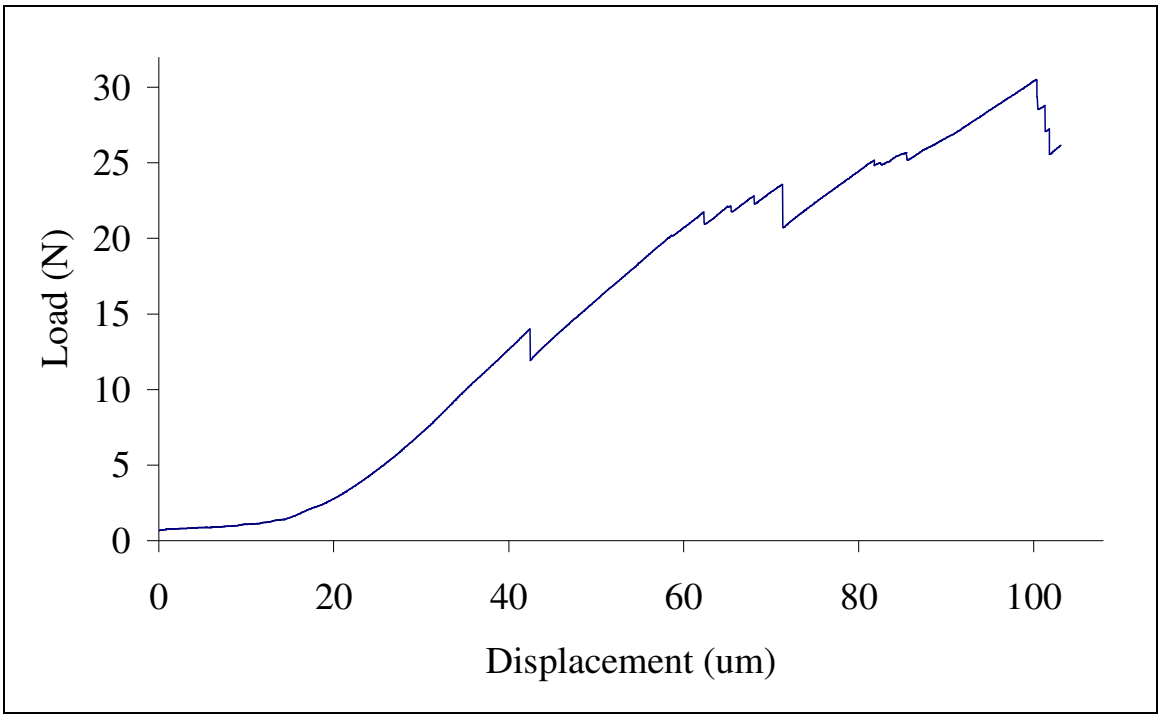

Figure 3.28 FPB partial delamination load vs. displacement curve

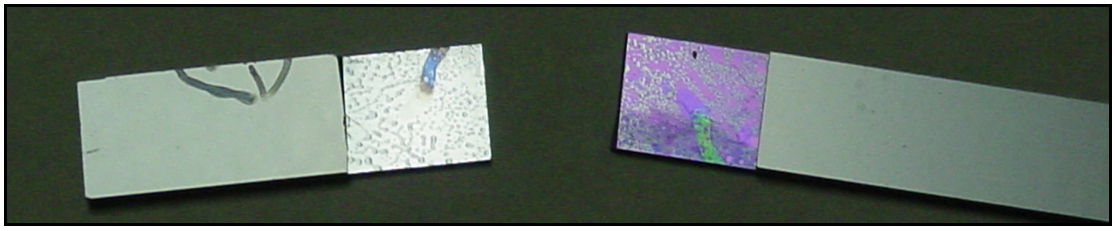

Figure 3.29 BPSG sample partial delamination

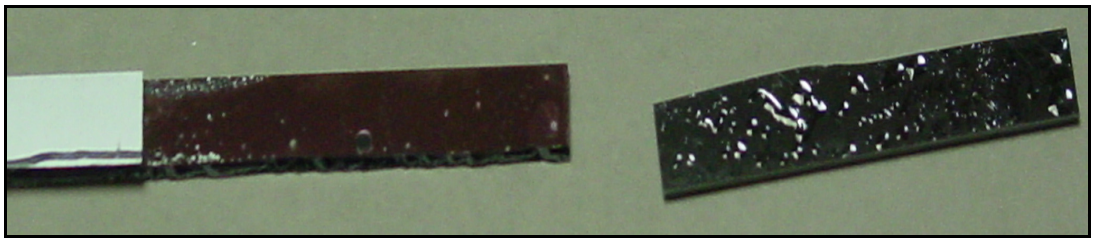

Figure 3.30 TEOS sample partial delamination

In this thesis 67 BPSG and 37 TEOS FPB samples were tested after the parameters for the FPB test were optimized to achieve delamination. Figure 3.31 shows the load vs. actuator curve profile of the delaminated sample for the BPSG wafer 22 sample test number 4 (BPSG22-4). The curve in figure 3.31 exhibits an ideal load vs. actuator displacement curve because it has linear loading, notch crack propagation at 29 N, and finally an abrupt load drop followed by a delamination plateau load of 61 N.

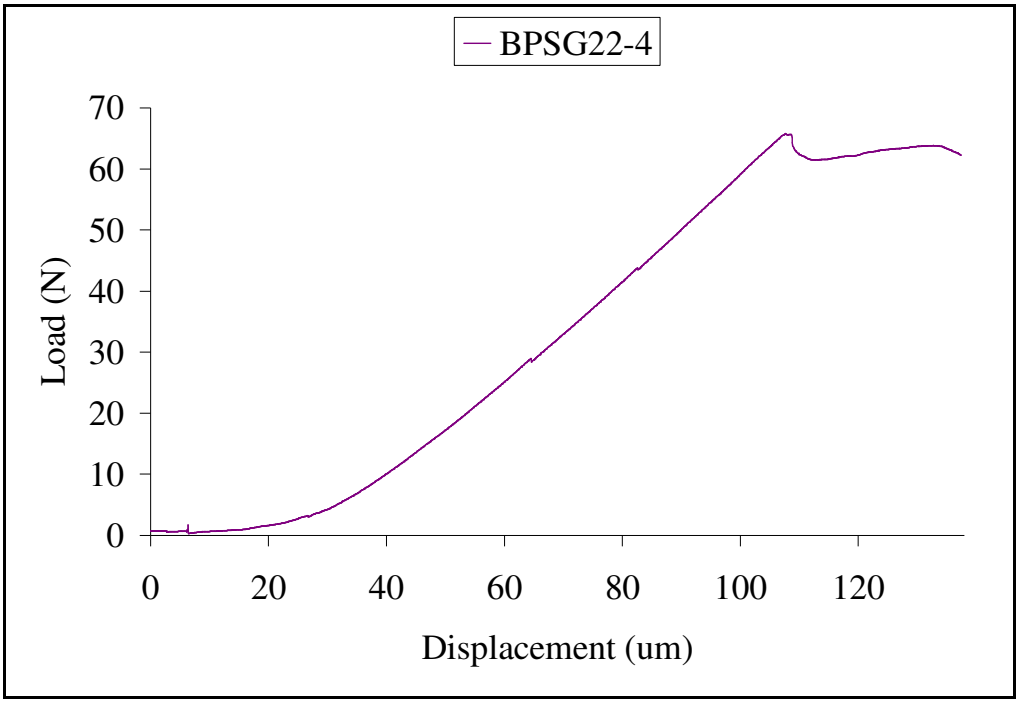

Figure 3.31 BPSG22-4 delamination curve

In figure 3.32 it can be seen that the Si surface is exposed from to the delaminated BPSG film. Figure 3.33 shows a magnified view of the BPSG22-4 sample surface revealing that the film was delaminated from the Si surface.

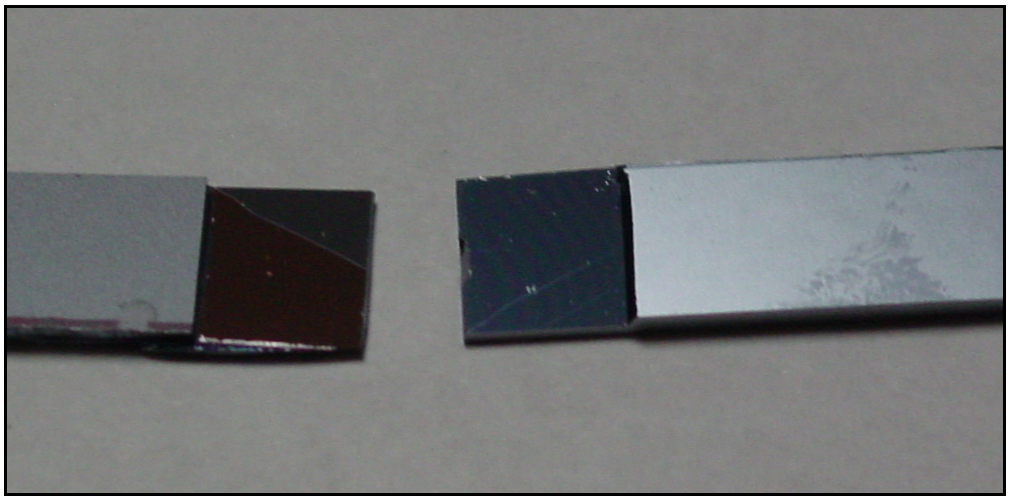

Figure 3.32 BPSG22-4 delamination

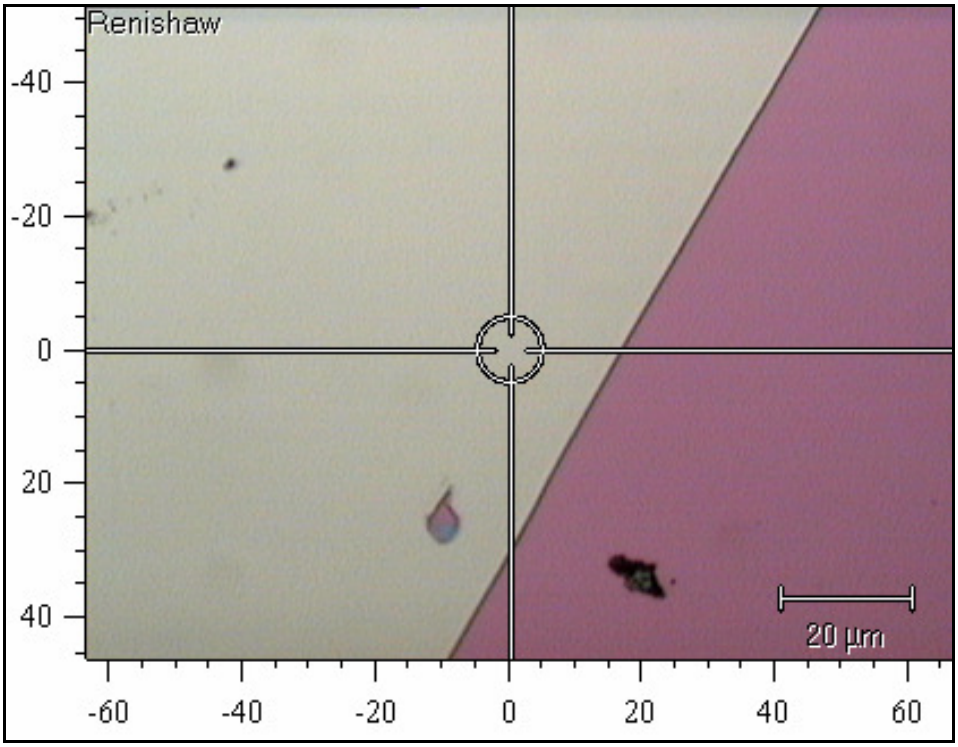

Figure 3.33 BPSG22-4 50X view of delamination

In this thesis Raman spectroscopy was performed on the all delaminated FPB test samples to verify that the low-k was completely delaminated from the surface exposing the underlying Si wafer surface. Depicted in figure 3.34 is a scan of standard Si calibration sample, where the peaks of 518 cm-1 - 521 cm-1 correspond to the material characterization of Si. Figure 3.35 depicts a scan of the BPSG22-4 delaminated surface. It can be observed that the peaks for figures 3.34 and 3.35 are identical, thus validating that the low-k film was completely delaminated from the underlying Si substrate.

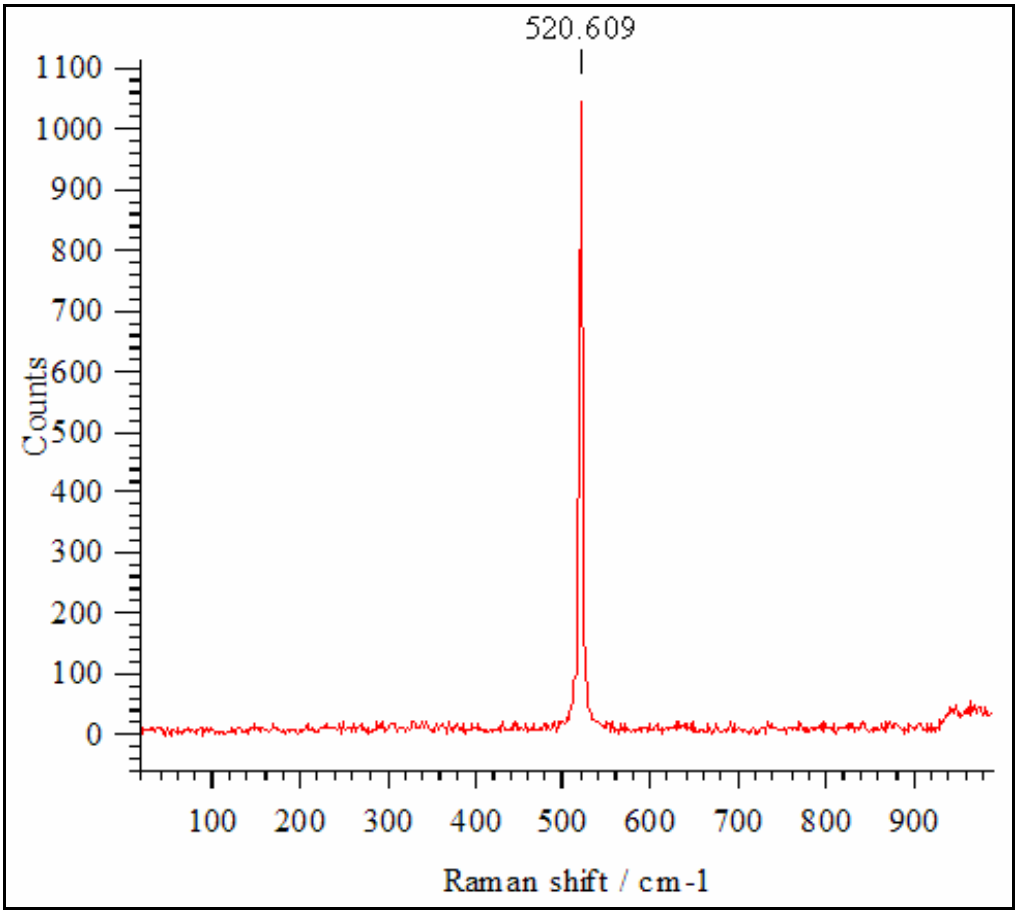

Figure 3.34 Raman spectroscopy calibration Si wafer

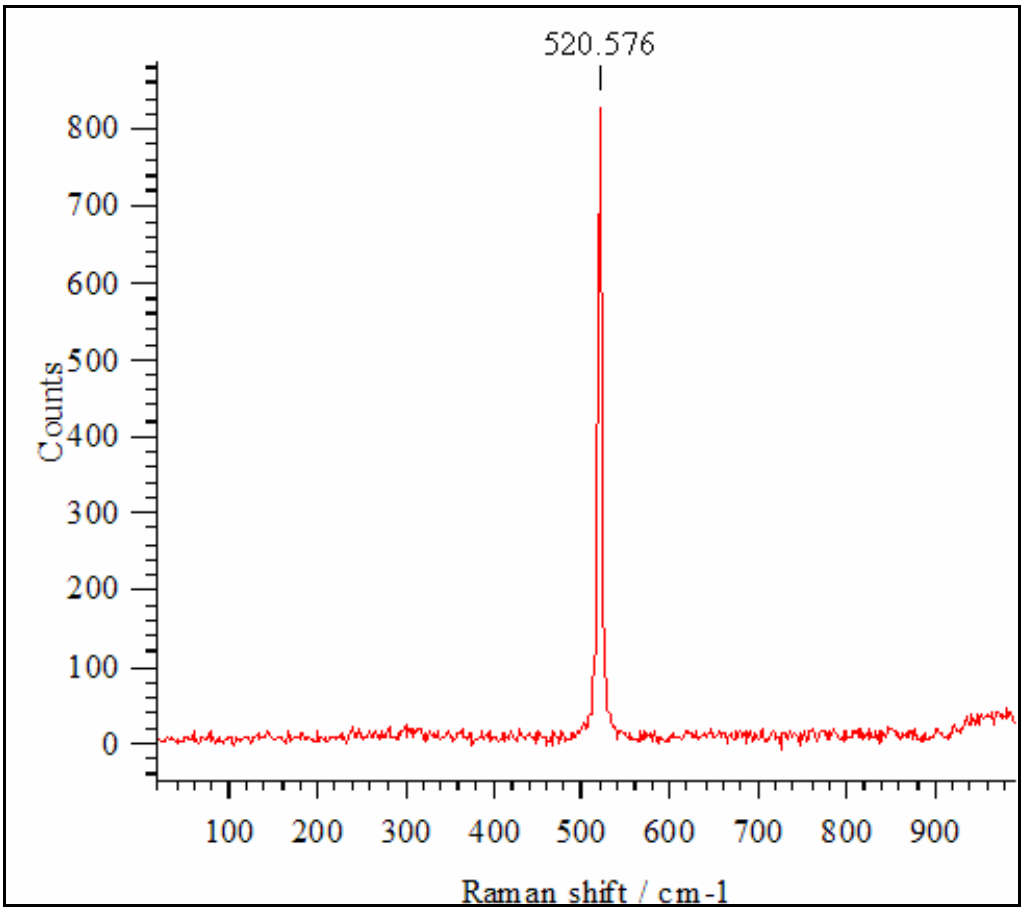

Figure 3.35 BPSG22-4 Raman spectroscopy of delamination

In this thesis only 10 of the 67 BPSG FPB samples tested were observed to delaminate. The average adhesion energy with the corresponding average plateau load of the delaminated BPSG samples is shown in figure 3.36. It can be seen in figure 3.36 that BPSG1-4, BPSG21-1, BPSG21-3, BPSG21-6, and BPSG21-7 all exhibited low adhesion energy values. It was observed that these low adhesion values were a result of partial delamination stemming from weak epoxy adhesion to the low-k BPSG film. However it can be seen that the BPSG samples that delaminated had consistent adhesion energy values.

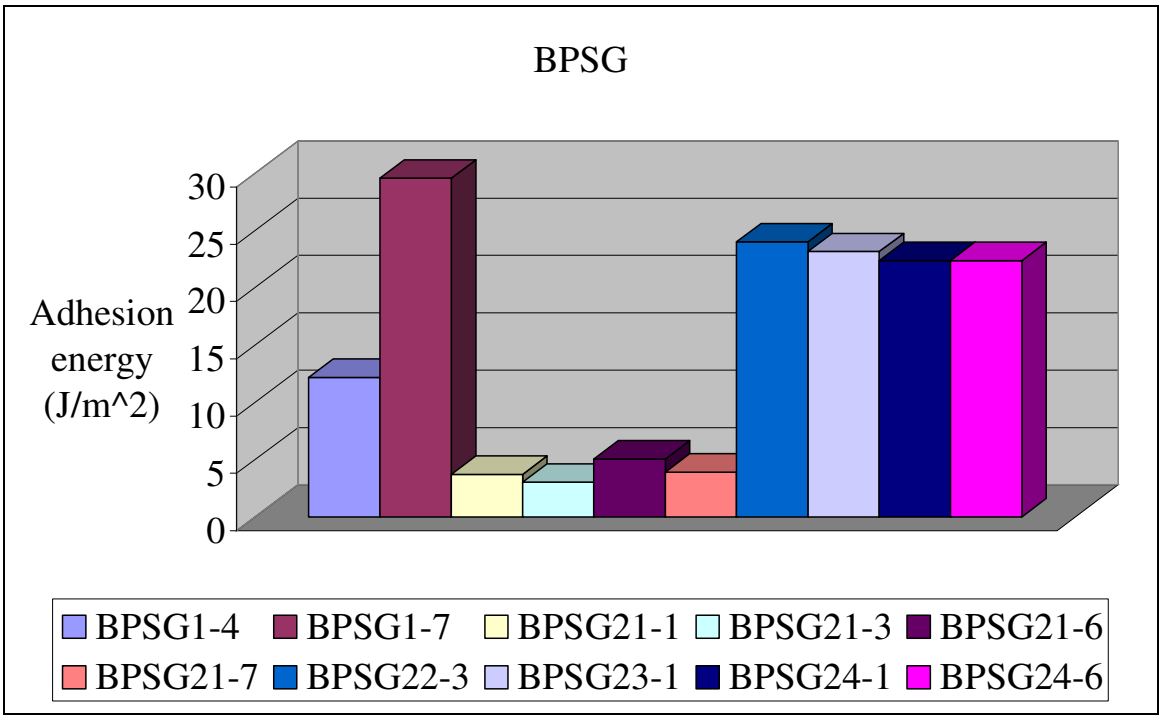

Figure 3.36 BPSG adhesion energy

The average adhesion energy value with the corresponding average plateau load of the delaminated BPSG samples is shown in table 3.1. The uncertainties in table 3.1 were calculated by the DTS Delaminator software.

Table 3.1 BPSG delamination

Low-k thin film	Plateau load (N)	Adhesion energy (J/m^2)
BPSG1-4	42.5703 ± 1.5831	12.1828 ± 0.3092
BPSG1-7	65.8295 ± 3.9541	29.5390 ± 0.5490
BPSG21-1	25.1499 ± 2.9583	3.7103 ± 0.1388
BPSG21-3	22.6832 ± 1.4198	3.0379 ± 0.8004
BPSG21-6	28.7871 ± 1.1170	5.0750 ± 0.2744
BPSG21-7	25.7207 ± 1.6649	3.9059 ± 0.8076
BPSG22-3	63.6350 ± 4.0507	23.9983 ± 0.5077
BPSG23-1	62.7778 ± 1.9729	23.1405 ± 0.5043
BPSG24-1	61.5126 ± 3.9421	22.3722 ± 0.4710
BPSG24-6	61.4900 ± 4.8933	22.3702 ± 0.4065

Figure 3.36 shows the load vs. actuator curve profile of delaminated sample for TEOS wafer 5, sample test number 8 (TEOS5-8). It can be observed that the delamination plateau load length appears short. The reduced plateau load length is due to premature fracture that occurred in the sample. In figure 3.37 it can be seen that the Si surface is exposed from the delaminated TEOS film. Figure 3.38 shows a magnified view of the TEOS5-8 sample surface revealing that the film was delaminated from the underlying Si substrate.

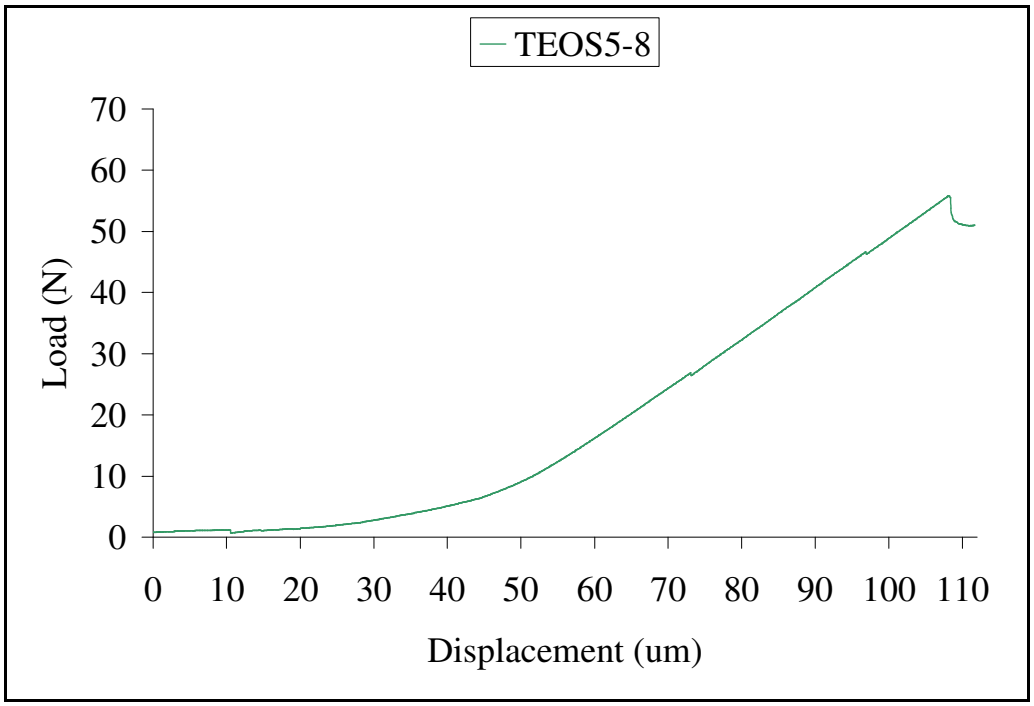

Figure 3.37 TEOS5-8 delamination curve

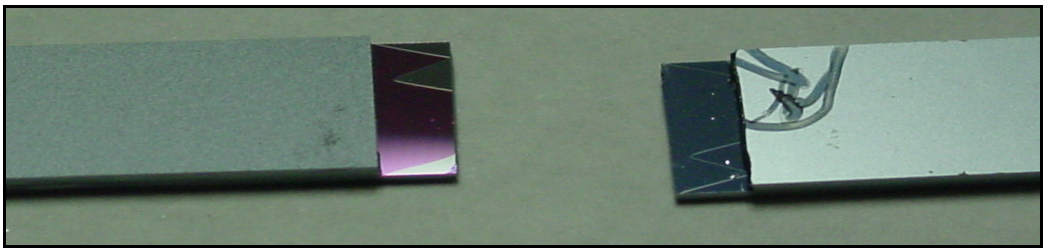

Figure 3.38 TEOS5-8 delaminated sample

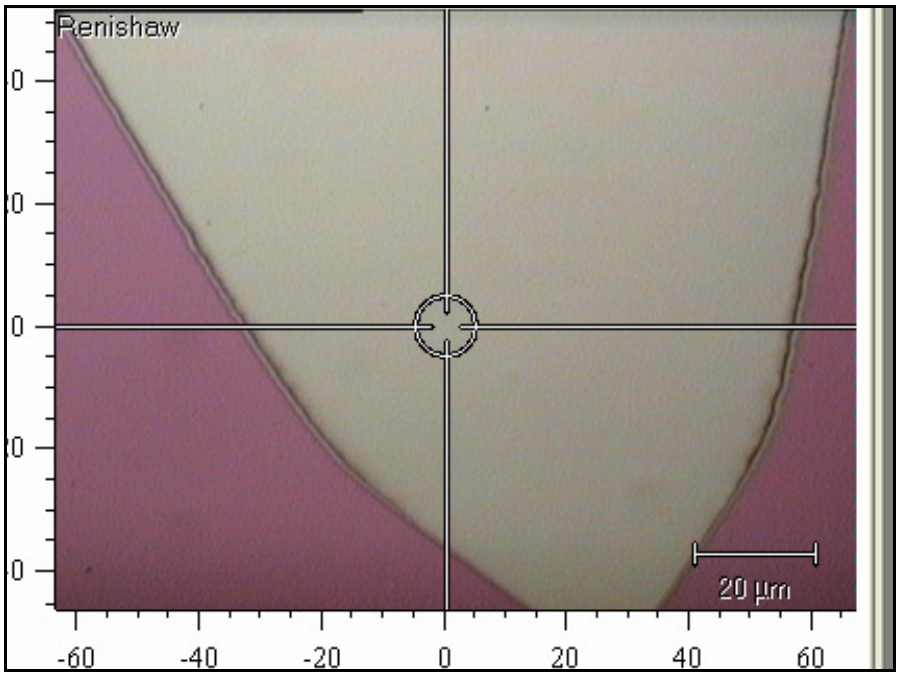

Figure 3.39 TEOS5-8 50X view of delamination

In this thesis only 3 of the 37 TEOS FPB samples tested were observed to delaminate. The average adhesion energy with the corresponding average plateau load of the delaminated TEOS samples is shown in table 3.2. The uncertainties in table 3.2 were calculated by the DTS Delaminator system software.

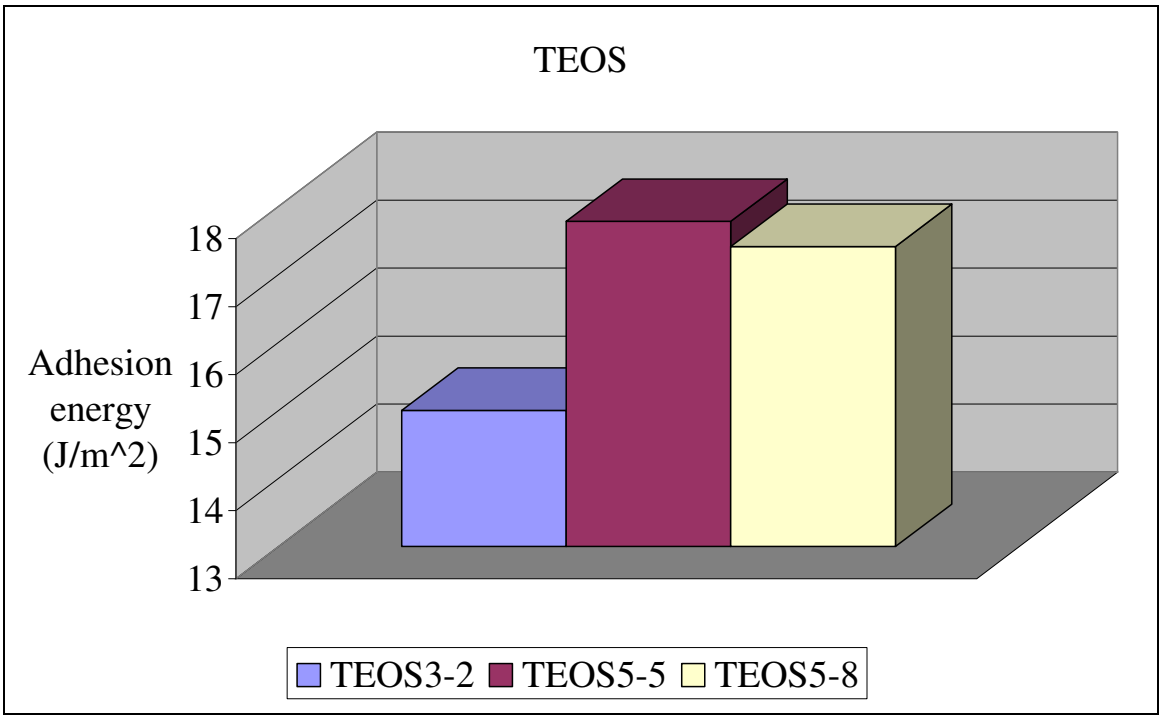

Figure 3.40 TEOS adhesion energy

Table 3.2 TEOS delamination

Low-k thin film	Plateau load (N)	Adhesion energy (J/m^2)
TEOS3-2	47.3926 ± 6.7239	15.0035 ± 0.4320
TEOS5-5	51.0301 ± 3.8358	17.7830 ± 0.5585
TEOS5-8	50.9668 ± 3.8474	17.4128 ± 0.5672

CHAPTER 4: EVALUATION OF ADHESION ENERGY FOR LOW DIELECTRIC CONSTANT THIN FILMS USING NANOSCRATCH TESTING

4.1 Introduction of scratch testing

Typically scratch testing involves applying an increasingly downward moving load across a material's surface until fracture occurs. Figure 4.1 illustrates a scratch test for measuring the scratch hardness, where F_T, F_N, and F_L are the measured lateral, tangential, and normal forces, respectively. Scratch hardness is defined as the track width of the scratched surface divided by the diameter of the scratch tip (Fischer-Cripps, 2002).

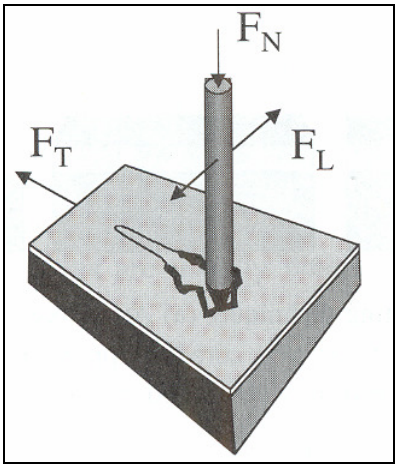

Figure 4.1 Configuration of a scratch test (Fischer-Cripps, 2002)

Scratch testing for measuring thin film adhesion is defined as the ability of a thin film to absorb energy until fracturing occurs in the form of delamination (Fischer-Cripps, 2002). The physical meanings of the results from scratch testing have long been

interpreted differently because different modes of fracture occur for varying indenter shapes and scratch velocities.

As scratch testing technologies continue to advance, the critical load for measuring of film fracture have begun to be measured by optical microscopy, acoustic emission (AE), and coefficient of friction (COF) force sensors. It is generally beneficial to use acoustic emissions and analysis of the coefficient of friction in conjunction to the optical microscopy if a scratch test system has them available. Figure 4.2 below shows the optical scratch test results of a multilayered Al/TiN/SiO 28 um thick film on a Si substrate.

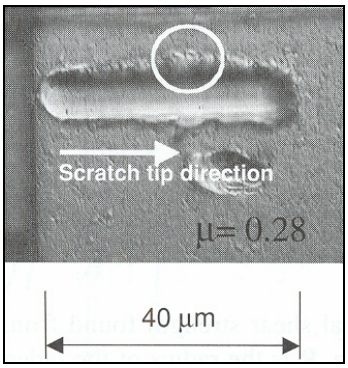

Figure 4.2 Scratch test on a multilayer thin film (Fischer-Cripps, 2002)

The coefficient of friction vs. scratch length graph in figure 4.3 corresponds with the scratch test results of the multilayered Al/TiN/SiO thin film in figure 4.2. The encircled area indicates a sudden change in the COF, showing when film fracture occurs.

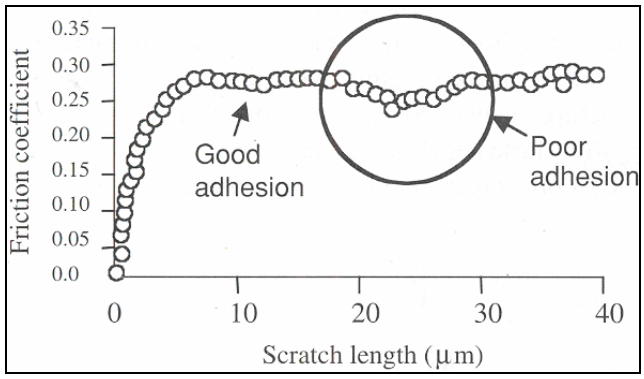

Figure 4.3 Coefficient of friction vs. scratch length (Fischer-Cripps, 2002)

4.2 Theoretical adhesion energy for nanoscratch testing

The critical resultant tangential and normal force needed to cause film delamination during a scratch test can be expressed in terms of work of adhesion. This work of adhesion is the work done to overcome the interfacial adhesion energy in order for film delamination to occur (Benjamin, 1960)

$$Pcr = \frac{A}{2}\left(\frac{2EW}{h}\right)^{\frac{1}{2}} \tag{4.1}$$

where Pcr is the resultant tangential and normal critical force. Rearranging equation 4.1, the critical load equation the work or adhesion energy with SI units of (J/m^2) is expressed as

$$W = 2\frac{Pcr^2\ h}{E\ A^2} \tag{4.2}$$

where h is the depth of the indenter in the thin film, E is the modulus of the thin film form the nanoindentation tests, and A is the projected area of the tip in contact with the film. The area A for a Berkovich indenter is (Fischer-Cripps, 2002)

$$A = 24.56\ h^2 \tag{4.3}$$

4.3 CETR Universal Tribometer system

In this thesis all nanoscratch tests were performed with the CETR Universal Tribometer at USF's advance materials lab. As seen in figure 4.4 the CETR Universal Tribometer carries acoustic emission (AE), tangential (Fz), and normal force (Fx) sensors that can detect the coefficient of friction during scratch tests. The CETR Universal Tribometer is also equipped with a FM-0.5 model sensor. The FM-0.5 model sensor is capable of dictating loads from 0.05 mN (5 g) - 5 N (500 g). The acoustic emission sensor provides an in-situ measurement of the indenter to indicate specific events in which the indenter head experiences abrupt changes during the load application.

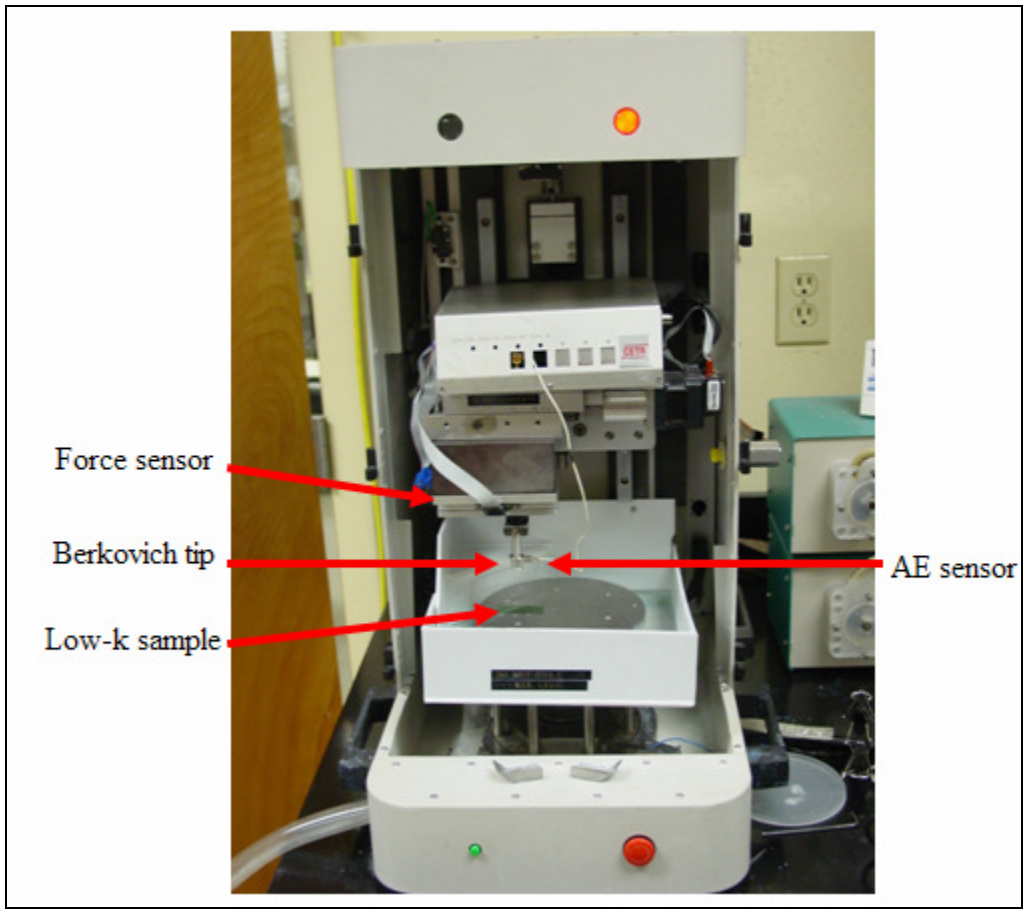

Figure 4.4 CETR Universal Tribometer

Figure 4.5 provides a clear view of the Berkovich tip and AE sensor attached to the nanoscratch tip housing. It should be noted the CETR Universal Tribometer software denotes the tangential (Fz) as negative, while this thesis denotes down forces as positive.

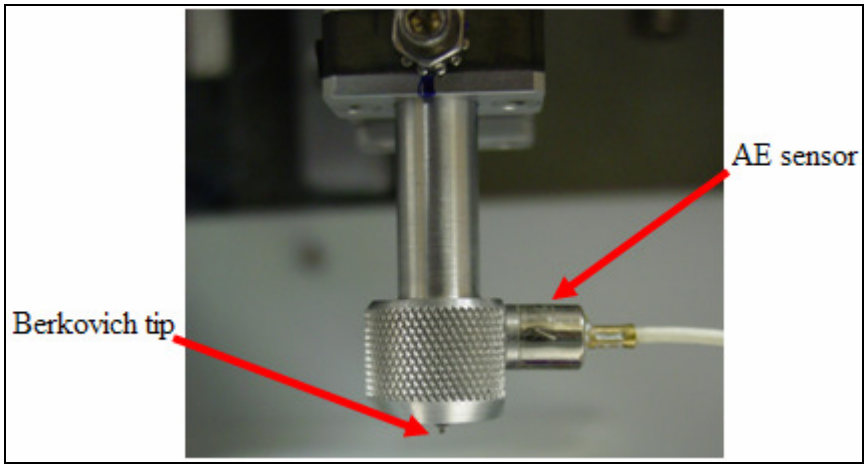

Figure 4.5 Scratch tip and AE sensor head

Due to the high cost of Berkovich indenter tips, the edge forward orientation was used for all scratch tests in this thesis. The edge forward tip orients the vertices of the tip parallel to the direction of the scratch path. Figure 4.6 is an illustration of the face forward orientation, which orients the tip face parallel to the direction of the scratch path. Studies have shown that scratch tests performed with a face forward orientation significantly decreased the life of the indenter and increase the risk damaging to the tip geometry (McAdams, 2006).

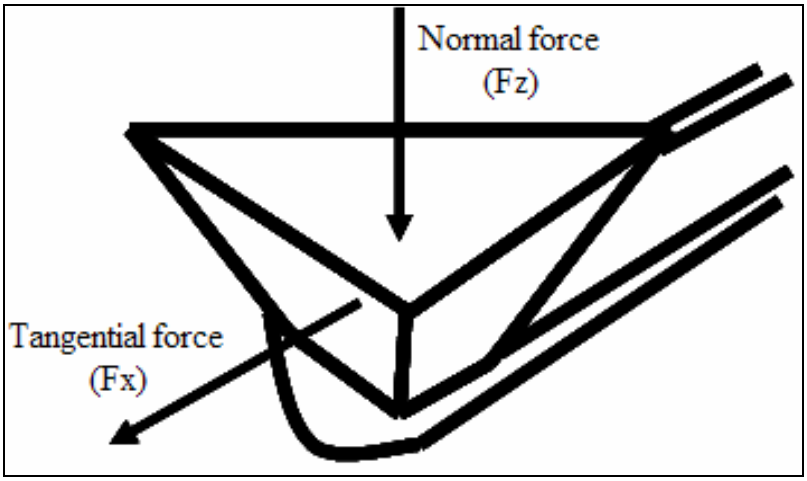

Figure 4.6 Face forward nanoscratch tip orientation

4.4 Nanoscratch sample preparation and test parameters

Sample preparation for nanoscratch testing is as simple as sample preparation for nanoindentation. First the nanoscratch test sample is prepared by scribing the low-k wafer into 30 mm X 42 mm rectangles. The sample is then individually adhered in place on the CETR Universal Tribometer steel stage and then tested as seen in figure 4.7.

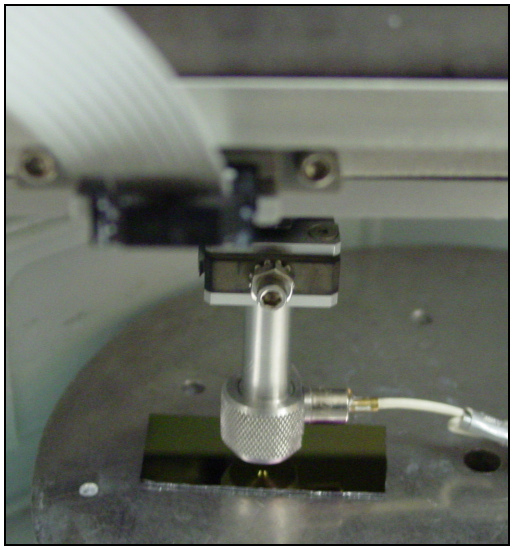

Figure 4.7 Nanoscratch sample setup

All nanoscratch tests performed in this thesis started with a 5 g (0.05 N) tip normal load and ended with a 105 g (1.05 N) tip normal load. Each scratch test length was kept constant at 37 mm. The nanoscratch test parameters in this thesis were governed by scratch length, initial tip normal load (Fz_i), final tip normal load (Fz_f), and tip load rate. For example as seen in table 4.1, with a the tip load rate of 0.01 N/s, nanoscratch test parameter 1 (NSCT1) needs a tip velocity of 0.352 mm/s to perform a 37 mm long scratch test which lasts 105 seconds; NSCT2, 3, 4 and were all determined this way. The table 4.1 below shows the variation in tip load rate, scratch tip velocity, and scratch test duration that was tested on each low-k film.

Table 4.1 Nanoscratch test (NSCT) parameters

Scratch test	Scratch length (mm)	Fz_i (N)	Fz_f (N)	Tip load rate (N/s)	Tip velocity (mm/s)	Scratch duration (s)
NSCT1	37	0.05	1.05	0.01	0.352	105
NSCT2	37	0.05	1.05	0.02	0.705	52.5
NSCT3	37	0.05	1.05	0.03	1.057	35
NSCT4	37	0.05	1.05	0.0555	2	18

Figure 4.8 below shows the Fx and Fz in-situ recording of a scratch test for NSCT1. The figure illustrates the 5 g Fz load (blue curve) and 0 g Fx load that is applied to the film for 5 seconds before the scratch test begins. This is done to ensure that the tip load is steady before scratching commences. Once the scratch test begins it can be seen

that the Fz increases to 105 g as the tip moves across the film surface. As a result of the Fz, the Fx experiences a frictional force which increases throughout the scratch test.

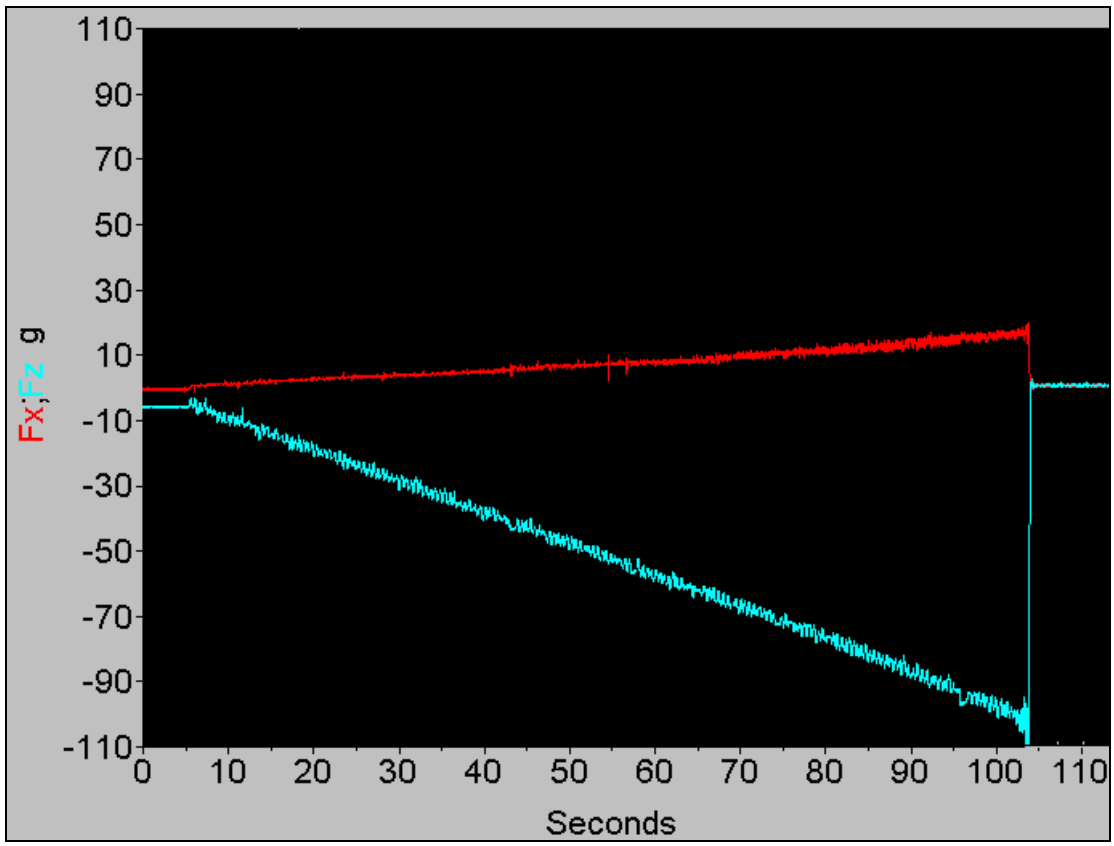

Figure 4.8 In-situ nanoscratch recording

4.5 Results and discussions of low-k thin film nanoscratch test results

Figure 4.9 shows the in-situ COF (red curve), AE (brown curve), Fx (blue curve), and Fz (blue curve) measurements for the BPSG low-k sample using nanoscratch test parameter 2 (NSCT2). The change in the AE signal curve in the shaded green region in figure 4.9 marks the instant that the surface of the BPSG film begins to be chipped off by the indenter at 12 – 14 seconds during the nanoscratch test. Figure 4.10 shows the SEM

(scanning electron microscope) of BPSG1 low-k film surface chipping which correspond with the shaded green region in figure 4.9.

The next AE signal change in the shaded red region in figure 4.9 marks the instant that delamination occurs in BPSG1 low-k film by the indenter at 20 – 22 seconds during the nanoscratch test. Figure 4.11 shows the SEM of the BPSG1 low-k film delamination which correspond with the shaded red region in figure 4.9.

Further along the nanoscratch test as the load approaches the maximum Fz value of 105 g, the shaded blue region in figure 4.9 marks the instant that the BPSG1 low-k film experiences complete delamination by the indenter at 25 – 49 seconds during the nanoscratch test. Figure 4.12 shows the SEM of exposed Si surface as a result of the BPSG1 low-k film experiencing complete delamination corresponding to the shaded blue region in figure 4.9.

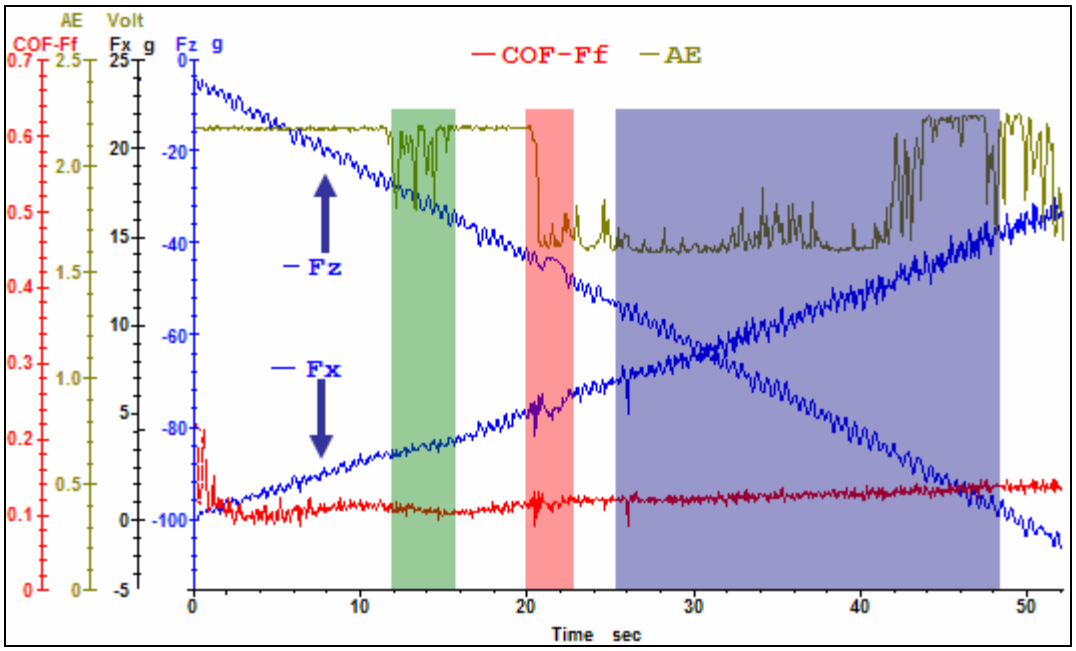

Figure 4.9 In-situ of the BPSG1 low-k film using NSCT2

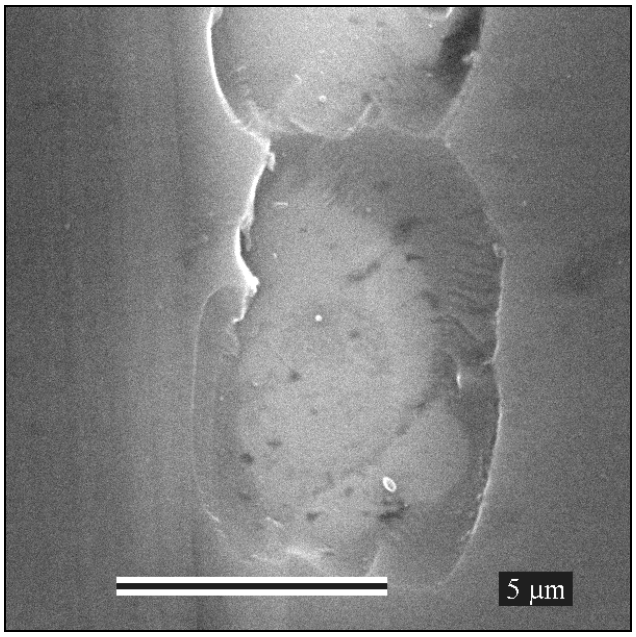

Figure 4.10 SEM of BPSG1 low-k film surface chipping

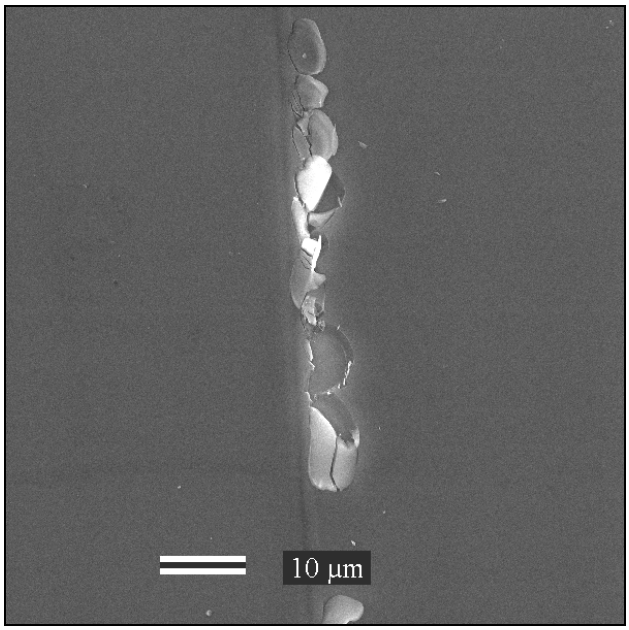

Figure 4.11 SEM of initial delamination of BPSG1 low-k film

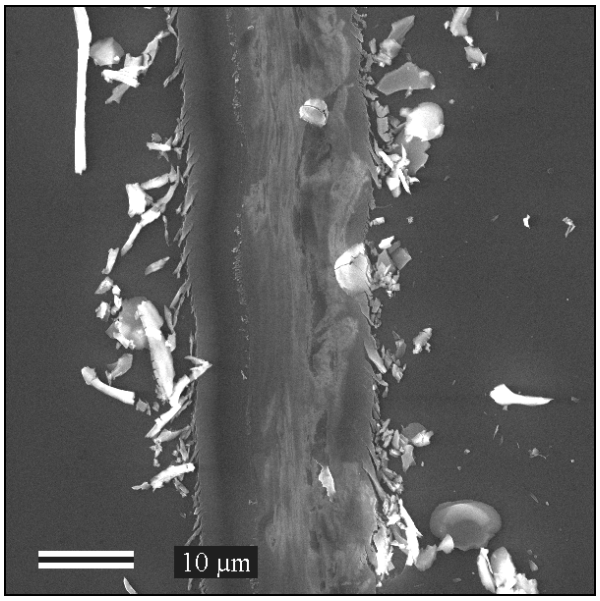

Figure 4.12 SEM of complete delamination of BPSG1 low-k film

Figure 4.13 depicts the in-situ COF (red curve), AE (brown curve), Fx (blue curve), and Fz (blue curve) measurements of the BPSG1 low-k sample using nanoscratch test parameter 4 (NSCT4). It can be seen that the AE signal was undisturbed during the nanoscratch test. Figure 4.13 also shows no clear COF, Fx, or Fz signal changes that mark the instances that the low-k film experiences surface chipping, delamination or complete delamination.

In this thesis it was observed that the NSCT2 was the only nanoscratch test parameter that consistently showed a clear COF, AE, Fx, and Fz signal change identifying instances when the BPSG and TEOS low-k thin films experienced surface chipping, delamination and complete delamination from the Si substrate. For this reason all adhesion energy measurements for nanoscratch testing where calculated from the Fx and Fz critical resultant loads obtained using NSCT2.

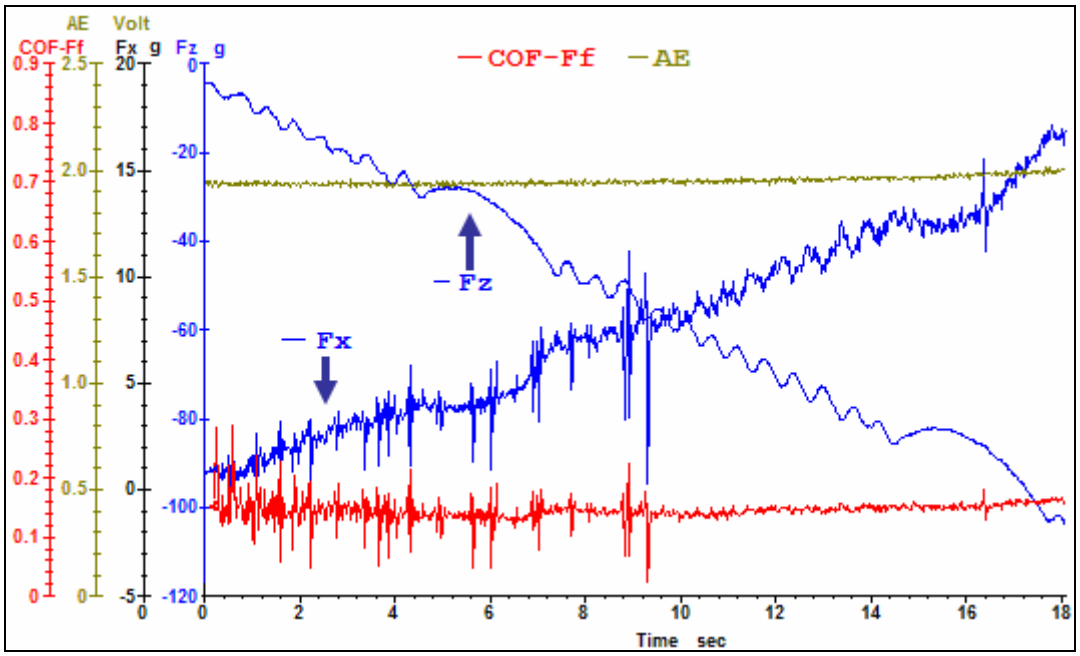

Figure 4.13 In-situ of the BPSG1 low-k film using NSCT4

Figures 4.14 and 4.15 show the nanoscratch test critical load and adhesion energy obtained using NSCT2 for the BPSG and TEOS low-k thin films. Figure 4.14 illustrates the consistent critical measurements obtained from the scratch test for the BPSG and TEOS. It can be observed that the adhesion energy of both the BPSG and TEOS did not change much. The consistency observed of the critical and adhesion energy for both the BPSG and TEOS is a result of the uniform material properties of the films and clarity of signal changes with using NSCT2 parameter for scratch tests.

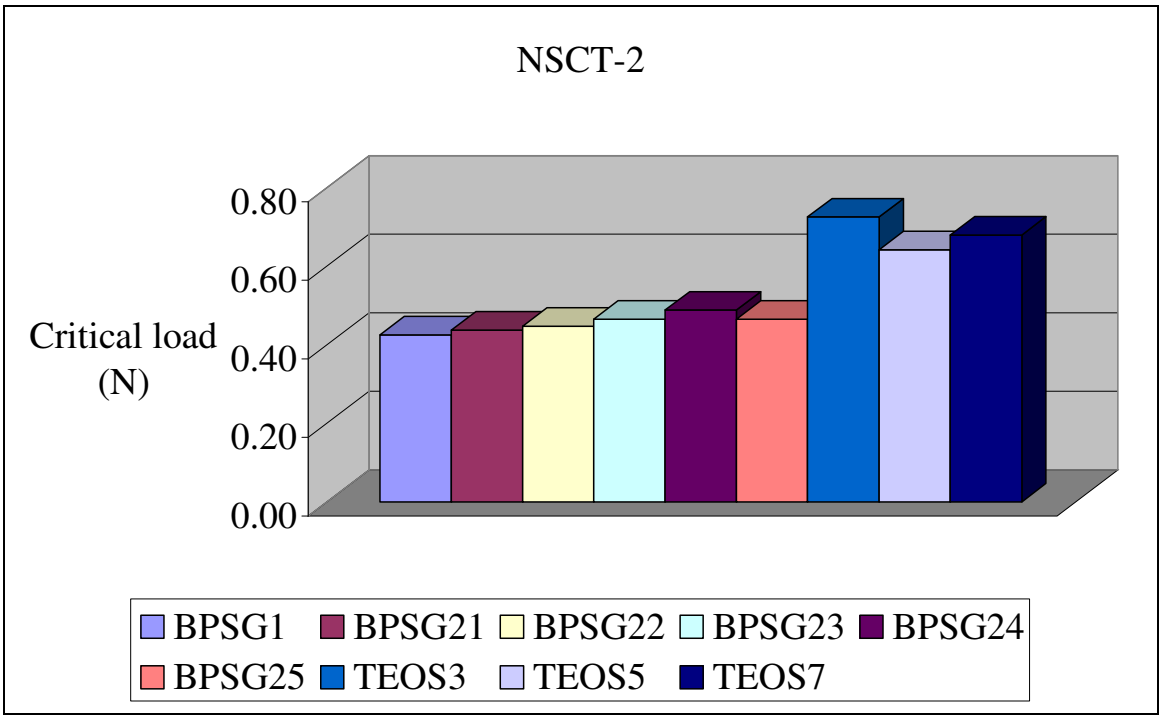

Figure 4.14 Nanoscratch test critical load for BPSG and TEOS low-k thin film

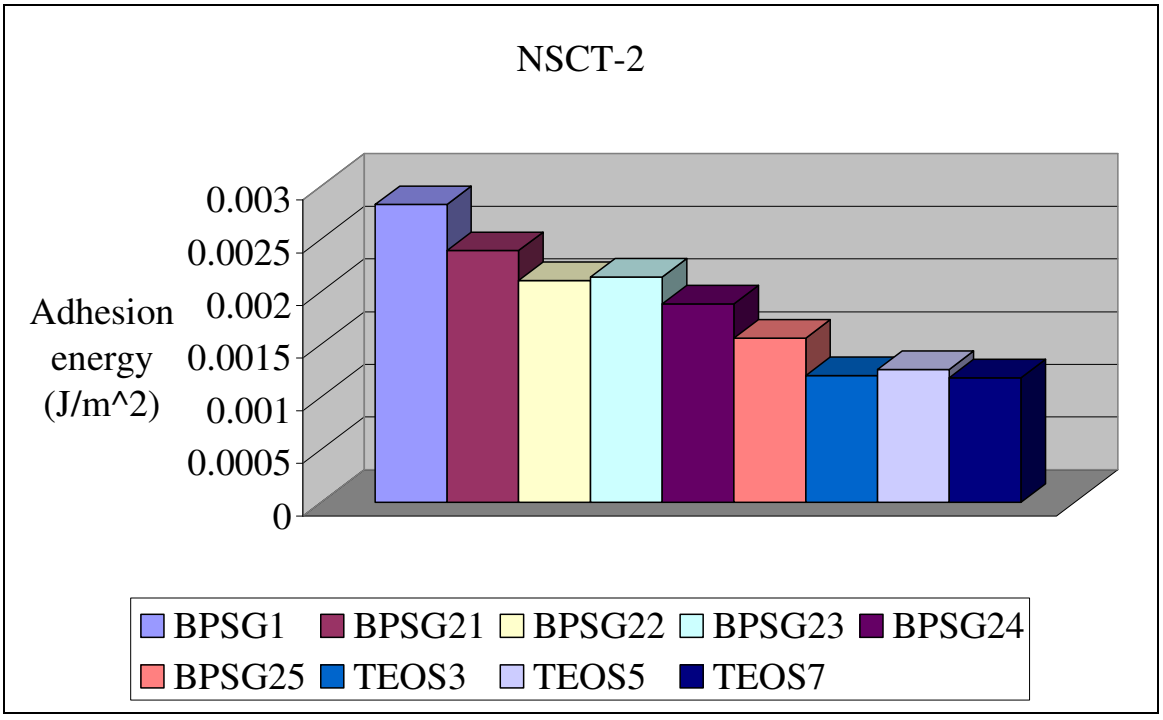

Figure 4.15 Nanoscratch test adhesion energy for BPSG and TEOS low-k thin film

The uncertainty values in table 4.2 were not provided by the CETR Universal Tribometer system, these values were calculated using the error propagation calculations discussed in section 4.6.

Table 4.2 Nanoscratch test critical load and adhesion energy for BPSG and TEOS low-k thin film

Low-k thin film	Pcr (N)	W (J/m^2)
BPSG1 NSCT2	0.4258 ± 0.0003	0.0028 ± 0.0006
BPSG21 NSCT2	0.4383 ± 0.0003	0.0024 ± 0.0005
BPSG22 NSCT2	0.4479 ± 0.0003	0.0021 ± 0.0004
BPSG23 NSCT2	0.4659 ± 0.0003	0.0021 ± 0.0004
BPSG24 NSCT2	0.4889 ± 0.0003	0.0019 ± 0.0001
BPSG25 NSCT2	0.4658 ± 0.0003	0.0016 ± 0.0003
TEOS3 NSCT2	0.7262 ± 0.0004	0.0012 ± 0.0001
TEOS5 NSCT2	0.6427 ± 0.0004	0.0013 ± 0.0002
TEOS7 NSCT2	0.6804 ± 0.0004	0.0012 ± 0.0001

4.6 Nanoscratch test error propagation

Error propagation for nanoscratch test results was performed to determine the resultant critical load and work of adhesion error. Using the error propagation equation (Dally, 1993)

$$dy = \sqrt{\left(\frac{\partial y}{\partial x_1} dx_1\right)^2 + \left(\frac{\partial y}{\partial x_2} dx_2\right)^2 + \ldots + \left(\frac{\partial y}{\partial x_n} dx_n\right)} \qquad (4.4)$$

$$Pcr = \sqrt{(Fx)^2 + (Fz)^2} \tag{4.5}$$

$$dFr = \sqrt{\left(\frac{\partial Fr}{\partial Fx} dFx\right)^2 + \left(\frac{\partial Fr}{\partial Fz} dFz\right)^2} \tag{4.6}$$

$$dFr = \sqrt{\left(\frac{1}{2}\left(Fx^2 + Fz^2\right)^{-\frac{1}{2}}(2\,Fx)(\Delta Fx)\right)^2 + \left(\frac{1}{2}\left(Fx^2 + Fz^2\right)^{-\frac{1}{2}}(2\,Fz)(\Delta Fz)\right)^2} \tag{4.7}$$

where ΔFx and ΔFz equal 0.00001 N.

The work of adhesion error propagation is

$$W = 2\frac{P_{cr}{}^2\, h}{E\, A^2} \tag{4.8}$$

$$dW = \sqrt{\left(\frac{\partial W}{\partial Pcr} dPcr\right)^2 + \left(\frac{\partial W}{\partial E} dE\right)^2 + \left(\frac{\partial W}{\partial h} dh\right)^2} \tag{4.9}$$

$$dW = \left[\left(\frac{4\,P_{cr}}{(24.56)^2 E\, h^3}\Delta Pcr\right)^2 + \left(\frac{-2\,P_{cr}{}^2}{(24.56)^2 E^2\, h^3}\Delta E\right)^2 + \left(\frac{-6\,P_{cr}{}^2}{(24.56)^2 E\, h^4}\Delta h\right)\right]^{\frac{1}{2}} \tag{4.10}$$

where $\Delta Pcr = 0.000355$ N , $\Delta E = 0.1\times 10^9$ Pa .

CHAPTER 5: THESIS CONCLUSION

5.1 Thesis summary

In this thesis the methodology behind indentation and nanoindentation for small scaled material was explained. Nanoindentation was used to evaluate the material properties of boro-phosphate-silicate glass (BPSG) and tetraethylorthosilicate (TEOS) low-k dielectric thins films deposited on Si substrates by chemical vapor deposition (CVD). The low-k material hardness and elastic modulus results obtained from the MTS Nano Indenter® XP showed that the films mechinacal properties were uniform throughout each dielectric wafer. The material properties obtained from nanoindentation tests were later used in determine the adhesion energy for nanoscratch testing performed on the low-k films.

Using the DTS Delaminator test system, four point bend (FPB) tests were performed to evaluate the adhesion energy for both BPSG and TEOS low-k films. The sample preparation procedures were optimized to promote interfacial delamination in FPB samples. New methods for epoxy application, FPB sample bonding, epoxy curing, and sample testing were observed reduce sample fracture and improve interfacial film delamination for the evaluation of low-k adhesion energy. A notch cut depth of 85 % of the top Si substrate also proved to be a very crucial parameter in achieving delamination in the samples. The adhesion results for both BPSG and TEOS were found to be

consistent for FPB samples that completely delaminated. However some samples experienced partial delamination caused by difficulties in applying a uniform thin layer of epoxy during in sample preparation.

The CETR Universal Tribometer was used for scratch testing because it carries acoustic emission (AE), tangential (Fz), and normal force (Fx) sensors that can detect the coefficient of friction during scratch tests. The edge forward tip orientation was selected to prevent tip damage during scratch testing. In addition, the nanoscratch testing parameter 2 (NSCT2) was observed to provide the best AE signal changes that corresponded with film delamination. The nanoscratch test results showed consistent adhesion energy measurements for the BPSG and TEOS films.

The adhesion energy for BPSG and TEOS low-k thin films using FPB testing ranged from 29.5390 J/m^2 - 3.0379 J/m^2. However adhesion energy for BPSG and TEOS low-k thin films using nanoscratch testing ranged from 0.0012 J/m^2 - 0.0028 J/m^2. This large disparity between FPB and nanoscratch test adhesion energy is due to the different failure modes by which delamination occurs in each test. As previously stated in section 1.7 in chapter 1 the interfacial fracture toughness (adhesion energy) between two materials is the work required to separate the materials from each other. During four point bending, the film to absorbed large bending forces which ultimately led to interfacial delamination. While in nanoscratch testing, the film only absorbed small a downward and shearing force causing chipping and buckling of the film which ultimately led to delamination.

5.2 Future work

In this thesis many FPB testing parameters and sample preparation procedures were optimized in order that achieve interfacial delamination. However even with these optimizations many samples experienced partial delamination and premature sample facture which made evaluating adhesion energy difficult. Improving the method of applying a uniformly thin epoxy layer may reduce the number partial delamination occurring in FPB samples. Along with improving epoxy application techniques, revising the clamping method for bonding the FPB sample should to be looked further. A rolling force applied to the sample may help reduce the amount of trapped air in the samples. One proposed method would be to put FPB sample into a vacuum after applying the epoxy. This would form very thin epoxy layer while completely removing any trapped air in the FPB sample.

Investigating the effects of notch cut depths of 90% to 95% were not looked at for fear that the dicing blade would cut into the interfacial layer. However if notch cut depths of 90% to 95% can be achieved in the FPB samples, it may greatly reduce the number of fractured samples by minimizing the abrupt strain release which occurs just before interfacial delamination. Lastly, the effects of micro cracks in regards to premature FPB sample fracture should be considered to reduce early sample fracturing.

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